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Digital Control of Static Var Compensator with Field Programmable Gate Array

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ABSTRACT

This paper is about real time simulation and implementation of FPGA Digital Control of Static VAR compensator for 750km lab model of artificial transmission line. In this paper, a new method of controlling SVC using Field Programmable Gate Array (FPGA) is suggested. FPGA controller is used to generate the firing pulses required to for Static Var Compensator. Pulses are synchronized with AC input; the delay of pulses determines the firing angle to driver circuit. The proposed control scheme has been realized using XILINX FPGA SPARTAN 2 XC2S200 and tested actual testing proves that these devices when installed, they keep the bus voltage same as reference voltage (sending-end voltage). The results are prominent and give a way for real-time implementation of the proposed control schemes. These control schemes are simulated for the real-time control along with real-time modeling and simulations.The results are prominent and give a way for real-time implementation.

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1. INTRODUCTION

FACTS devices like SVC can supply or absorb the reactive power in the transmission line, which helps in achieving better economy of power transfer [1]. In deregulated environment reactive power generated by transmission line is one of the important aspects to be considered. Reactive current control through SVC considering load power factor discussed in [2]. SVC control system is implemented in [3]. FACTS devices like SVC can supply or absorb the reactive power in the transmission line, which helps in achieving better economy of power transfer Shunt controllers inject current into the system at the point where they are connected. They can be used as a good way to control the voltage in and around the point of connection by injecting active or reactive current into the system.

In this paper artificial transmission line of 750Km ($\lambda/8$) is simulated and tested. SVC (TCR+FC) is placed at the receiving end. The receiving end voltage fluctuations were observed for different loads. It was found for light load, receiving end-voltage is greater than sending end-voltage ($V_R > V_S$) and for heavy load receiving end-voltage is less than sending endvoltage ($V_R < V_S$) [10] [11]. The firing angle for SVC and phase angle for control for various loading conditions to make the receiving end voltage equal to sending end voltage. In this work FPGA base digital firing scheme is implemented to achieve the better control. The advantages of digital controllers are less external passive components, less sensitive to temperature variation, high efficiencyand reconfigurability.The micro-processor based control schemeused in [3] have the advantages of flexibility, higher reliability and lower cost, but the demanding control requirements of modern power conditioning systems will overload most general purpose micro-processors and the computing speed of microprocessor limits the use of microprocessor in complex algorithms. Digital Signal Processors (DSPs) and Microcontrollers are used for digital control applications.

But DSPs and Microcontrollers can no longer keep pace with the new generation of applications that require not just higher performance also more flexible without increasing cost and resources [4].

The simplicity and programmability of FPGA make it the most favorable choice for prototyping digital systems. Very Large Scale Integration (VLSI) technology and Electronic Design Automation (EDA) techniques created an opportunity for the development of complex and compact high-performance controllers [5]. FPGA is a Programmable Device, compressing thousands of logic gates in a single chip and some of them can be combined to form a Configurable Logic Block (CLB). FPGA benefits of using portable high level Hardware Description Languages (HDLs). It allows concurrent operation, reduced time, easy and fast circuit modification and low cost even for complex circuits. It also maximizes operational performance to achieve high efficiency and power quality while simultaneously allows the rapid prototyping of digital controllers in ASICs [6].

2. OPERATING PRINCIPLE OF SVC

A shunt connected SVC (static var generator or absorber) whose output is adjusted to exchange capacitive or inductive current so as to maintain or control specific parameters of the electrical power system (typically bus voltage) [12] [13]. It is basically a fixed capacitor, thyristor controlled reactor type of Var compensator. The basic elements of TCR are a reactor in series with a bi-directional thyristor switch. The thyristor conducts on alternate halfcycles of the supply frequency depending on the firing angle 'α', which is measured from zero crossing of voltage. Full conduction is obtained with a firing angle of 90^o. The main concept behind controlling TCR is the control of the firing time of the thyristor to control the current in the reactor, thus controlling the reactive power absorbed by the TCR.Using appropriate switching controls, the var output can be controlled continuously from maximum capacitive to maximum inductive output at a given network voltage. The TCR +FC controller used as an elementary single-phase Thyristor controlled reactor (TCR) shown in Fig.1, consists of a fixed reactor of inductance L and a two anti parallel SCRs. The device brought into conduction by application of synchronized gate pulses to SCRs. In addition, being a current operated device it will automatically block immediately after the ac current crosses zero, unless the gate signal reapplied. The current in the reactor can be controlled from maximum (SCR closed) to zero (SCR open) by the method of firing delay angle control. That is, the SCR conduction delayed with respect to the peck of the applied voltage in each half-cycle, and thus the duration of the current conduction interval is controlled.

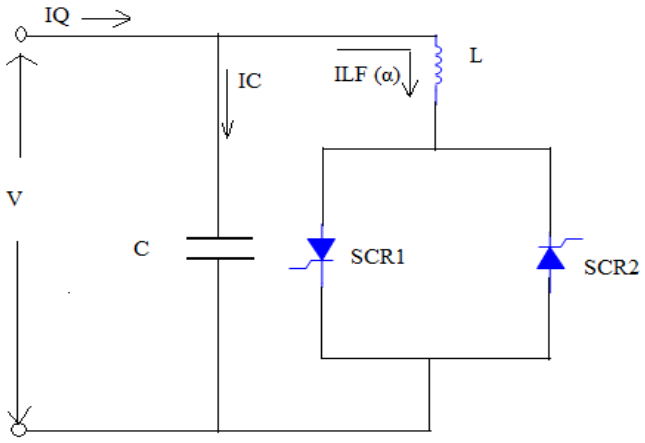

Figure 1. Basic Thyristor Controlled Reactor SVC (TCR+FC)

When the gating of the SCR is delayed by an angle α ($0 \le \alpha \le \pi/2$) with respect to the crest of the voltage, the current in the reactor can be expressed as follows

$$i_L = \frac{1}{L}\int_{\alpha}^{\omega t} V(t)dt = \frac{V}{\omega L}(Sin(\omega t) - Sin\,\alpha) \quad (1)$$

The amplitude $I_{LF}(\alpha)$ of the fundamental reactor current is expressed as a function of angle α

$$I_{LF}(\alpha) = \frac{V}{\omega L} * \left(1 - \left(\frac{2}{\pi}\right)\alpha - \left(\frac{1}{\pi}\right)\sin(2\alpha)\right) \quad (2)$$

Where V is the amplitude of the applied voltage, L is the inductance of the Thyristor-controlled reactor, and ω is the angular frequency of the applied voltage.

The effective reactance admittance, as a function of angle α is given as

$$B_L(\alpha) = \frac{1}{\omega L} * \left(1 - \left(\frac{2}{\pi}\right)\alpha - \left(\frac{1}{\pi}\right)sin(2\alpha)\right) \quad (3)$$

The admittance $B_L(\alpha)$ varies with α in the same manner as the fundamental current $I_{LF}(\alpha)$. The meaning of equation (3) is that at each delay angle an effective admittance $B_L(\alpha)$ can be defined which determines the magnitude of the fundamental current $I_{LF}(\alpha)$ [12].

3. ANALYSIS AND HARDWARE IMPLEMENTATION

The primary objective is to control the reactive power of line and not the reactive power of load hence only resistive load is considered. An available scale down Artificial transmission λ/8 - line model is used which is available in laboratory having 4 π line segments with 750 km distributed parameters .The line inductance = 0.1mH /km, Capacitance = 0.10 μf/km, Line resistance = 0.001Ω /km. and Surge Impedance $Zc = \sqrt{(L/C)}$ = 31.6 Ω, Supply Voltage = 230 V-50 Hz. In most of the transmission lines Ferranti effect is predominant and receiving end voltage is greater than that of the sending end voltage at light load. Therefore the shunt reactor in installed in the line for excess VARs in line. The value of reactance required is evaluated as shown below:

$$X_L = \frac{Sin\,\beta l}{(1-Cos\beta l)} * Z_C \quad \text{and} \quad \beta = 2*\pi*f\sqrt{L*C}; \quad (4)$$

Thus inductive reactance required for compensation under no load is 59.69Ω. Therefore L= .19H and value of Capacitance is chosen based on required leading VArs = 6 μf.Total power system shown in Figure 2.

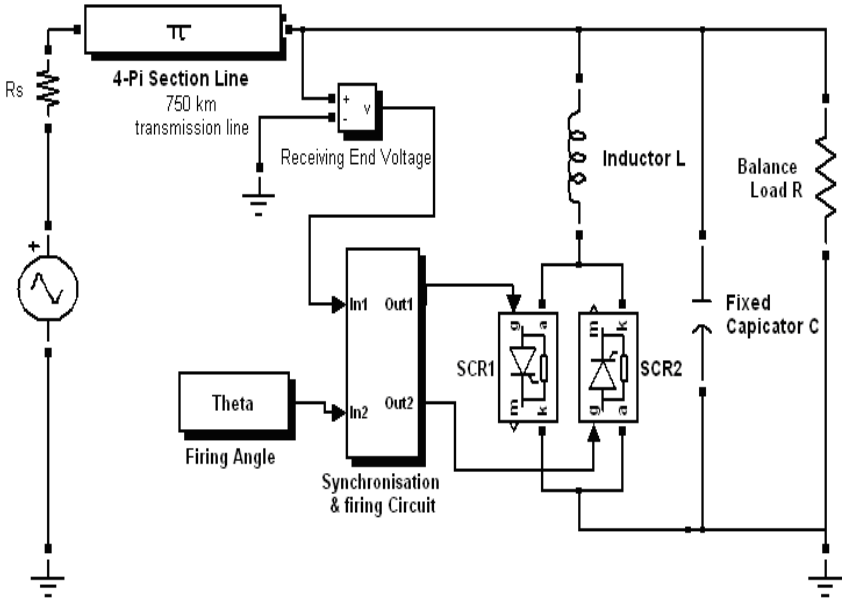

Figure 2. SVC Connections in The System

3.1. Methodology Used

FPGA kit (Spartan 2) is used as a hardware platform in this work. VHDL language is use as a software development tools for the XC2S200 programming. Xilinx is software that provides an environment and software tool set to users of development of project, this is the software platform in this work,which generates required firing angle for SVC . The firing angle control of SVC is designed and the firing angles are varied manually for various loading conditions to make the receiving end voltage equal to sending end voltage. All the results thus obtained in open loop as well as in closed loop with feed back controller are. Based on observed results, controller is designed to achieve the firing angles for SVC such that it maintains a flat voltage profile at the receiving end.To have full control over the firing angle of the SCRs (from 0 to 90 degree) using cosine wave reference, it is necessary to precisely detect the zero crossing of the sinusoidal input. Conventional zero crossing detectors cannot distinguish between start of positive half cycle or negative half cycles [6]. Schematic of the zero crossing circuit that was implemented is shown in Figure 3.

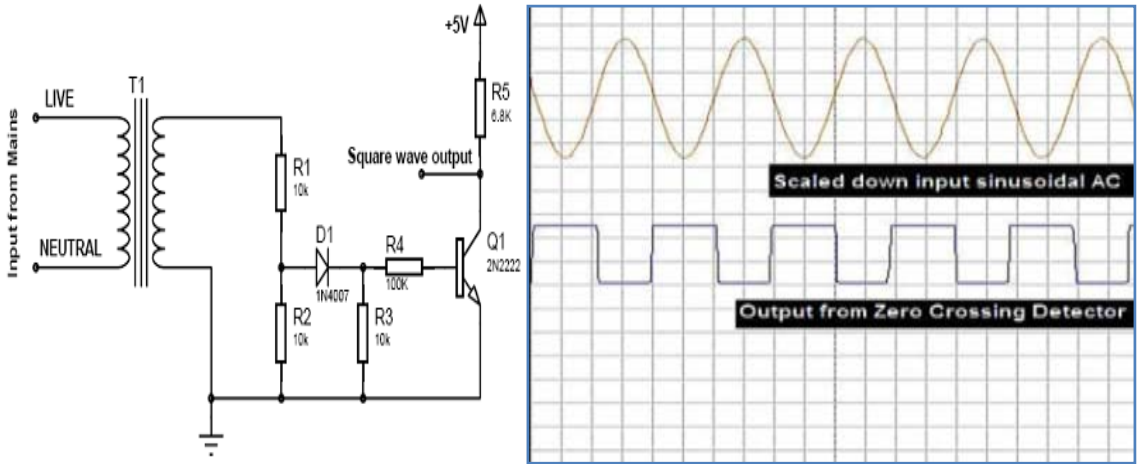

Figure 3. ZCD and Wave Forms of ZCD

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3.2. The Firmware

Firmware of the system is written entirely in VHDL language due to its friendly execution on XILINX SPARTAN 2 XC2S200 FPGA Board. The FPGA board used in this proposed design has 'VHDL friendly' architecture with a large logic array to store the variables in circuit for faster access [8] [9]. Whenever zero crossing is detected on the mains power line, counter start counting the latest values of firing delay and firing angle are used to generate gate triggering pulses. Keyboard 4 Switches combination reading is converted into the firing angle. The relationship between keyboard output and firing angle is given in $\alpha = (180/15)*$ Number entered as Input through keyboard

As keyboard of XILINX SPARTAN 2 XC2S200 FPGA Board use is of 4-bit resolution hence the maximum value from the keyboard with 15(i.e.$(1111)_2$). Keyboard reading is converted into a delay after which firing pulse is to be generated.

3.3. Driver Circuitry

The triggering pulse is generated at the output pin of XILINX SPARTAN 2 XC2S200 FPGA board is 4.8V, this pulse is provided to the input of optocoupler which convert this small voltage and current into appropriate driving voltage and current and apply it to the gate of the thyristor as a result thyristor gets fired [5].With the variation in the keyboard switches combination delay is inserted in the generation of triggering pulse with respect to sinusoidal voltage which is known as firing angle. Hence when this pulse is provided to the optocoupler it triggers the thyristor. we can change the keyboard switches combination by varying the switches position there by changing the firing angle as a result controlled output power is achieved at the output **.**Synthesis is the process of generating RTL view of the HDL design, so after synthesis the generated RTL View of the FPGA Controller as shown in Figure 5.

3.3. Results

For the experimental setup FPGA kit. (Spartan 2 family device "XC2S200") is use following are the result obtained during experimentation.Output of clock divider network is of 761Hz. Figure. 6.1 show the result of clock divider network

The supply frequency 50Hz

$$T = \frac{1}{50HZ} \qquad T = 0.02sec$$
$$T = T1(Positive\ Cycle) + T2\ (Negative\ Cycle)$$
$$T = 0.1(Positive\ Cycle) + 0.1(Negative\ Cycle)$$

Now in the work we have 4 switches we can have 15 combinations, so we can divide one half cycle into 12 delay position.

One Step Delay in Deg = 180˚/15
One Step Delay in Deg = 12˚
One Step Delay in time= 0.01Sec/15 (For one Cycle)
One Step Delay in time= 0.01Sec/15
One Step Delay in time= 666.666µs

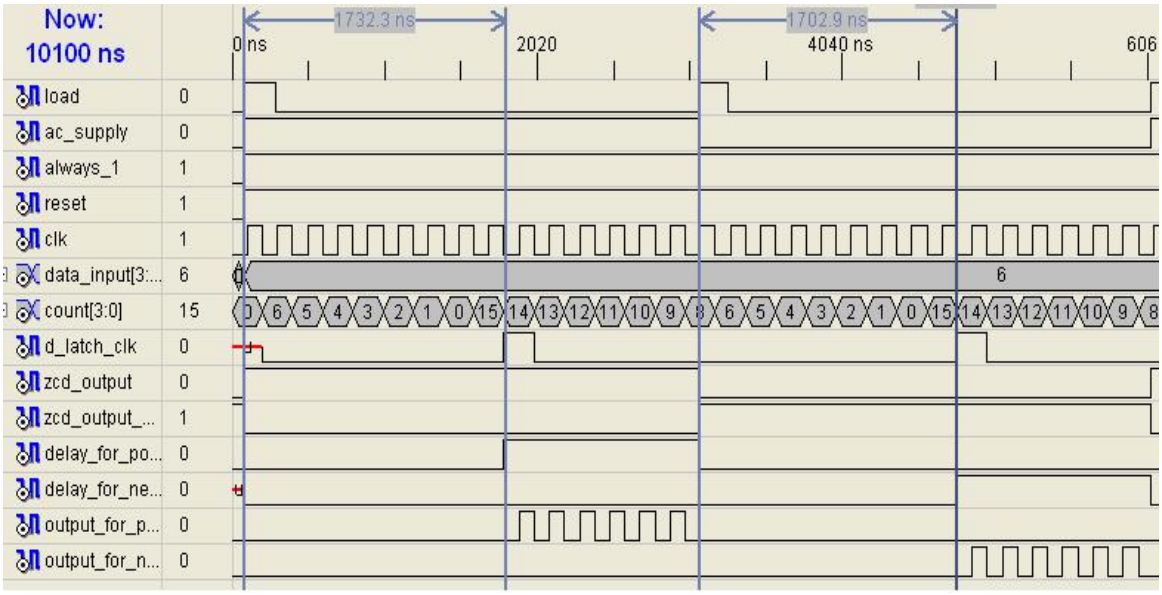


Figure 4. Simulation Result Delay Generated For Count Value 6 For Both Half Cycles of AC in Put

The firing angle control of SVC is designed and the firing angles are varied manually for various loading conditions to make the receiving end voltage equal to sending end voltage. All the results thus obtained in open loop. Keyboard switches are use for controlling the firing angle there by control of the firing time of the thyristor to control the current in the reactor, thus controlling the reactive power absorbed by the TCR. Using appropriate switching controls, the VAr output can be controlled continuously from maximum capacitive to maximum inductive output at a given network voltage.Time delay generation with count value 0101 (six) is shown in fig .4 Hence four input from 0000 to 1111 generated delay time is shown in Table 1.The design is an economical, easy to realize, user friendly and is fully isolated from main supply line at both the input and output stages to nullify the effect of noise and electromagnetic interference over the mains power line. Design is of universal nature that can be used with 50 Hz as well as with 60 Hz power distribution standards. The code is simulated using XILINX 8.2 ISE software and this code is dumped into XILINX SPARTAN 2 XC2S200 FPGA Board. Keyboard switches are use for controlling the delaye there by control the firing angle of two antiparallel thyrister (SVC), which is placed at the receiving endof the 750 km aritfical transmission line available in the laboratory.

Table 1. Reading for Trigger Pulse Form FPGA Pin

Sr.No.	Input Data	Delay(ms)	No. Of Output Pulses
0.	0000	0.0000	13
1.	0001	0.6666	12
2.	0010	1.3333	11
3.	0011	1.9998	10
4.	0100	2.6664	9
5.	0101	3.3333	8
6.	0110	4.0000	7
7.	0111	4.6666	6
8.	1000	5.3333	5
9.	1001	6.0000	4
10.	1010	6.6666	3
11.	1011	7.3333	2
12.	1100	8.0000	1
13.	1101	8.6666	Zero
14.	1110	9.3333	Zero
15.	1111	1.0000	Zero

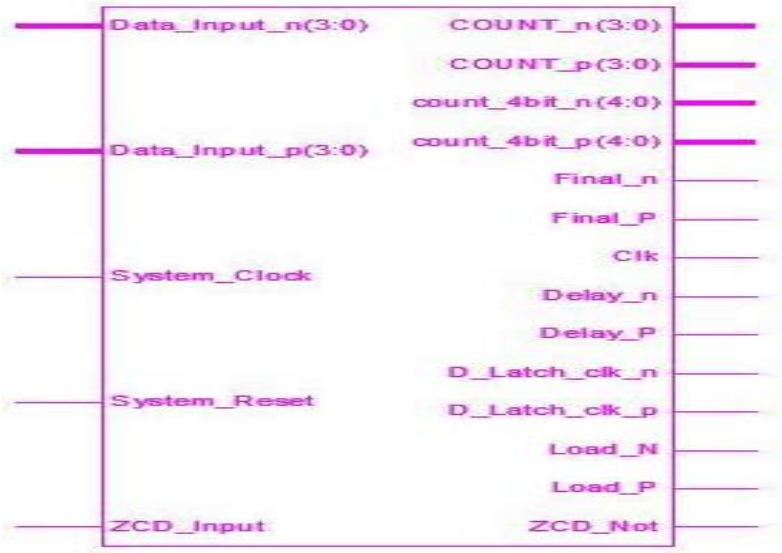
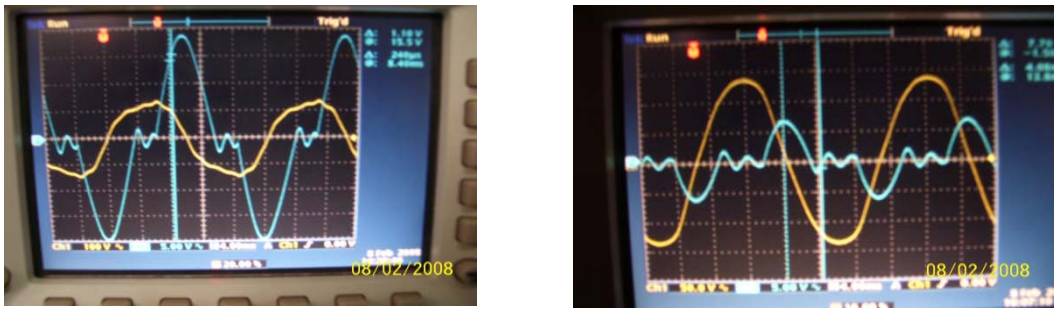


Figure 5. Top Module RTL View of FPGA Controller



(a) (b)

Figure 6. Inductor Current Wave Form (a) For Firing Angle $\alpha=100^0$ (b) For Firing Angle $\alpha=150$

4. CONCLUSION

Triggeriggring of SVC controlled by the delay period with FPGA to trigger the thyristors thereby effective suspecentance of SVC is control. The result obtained by proposed method shows the excellent performance and can be easily implement for real time control of power system. Close loop system control can be achive with 4-bit ADC .The method is fully software upgradable to alter the design to drive more devices. Components used to implement this proposed design are also simple. It can be implemented with cheap and all-time available components providing a ready-to-use solution.

REFERENCES

[1] L.Dong, et al, "A Reconfigurable FACTS System for University Laboratories*", IEEE Transactions on Power Systems, vol. 19*, no. 1, February 2004.

[2] Samesh K.M.Kodsi, et al, "Reactive current control through SVC for load power factor correction", *Electric Power System Research* pp.701-708. 2006

[3] H. M. EL-Bolok, M. E. Masoud, and M. M. Mahmoud, "A Microprocessor-Based Adaptive Power FactorCorrector for Nonlinear Loads", *IEEE Transactions on Industrial Electronics,* vol. *31,* no. i ,pp. 77-81 Feb 1990.

[4] Murugesan S. and Kameswara C, "Simple adaptive analog and Digital trigger circuits for thyristors working under wide range of Supply frequency,*" IEEE Trans. Ind. Electron. Contr. Instrum., IECI-24* (1), pp. 46–49, 1977.

[5] Gupta S.C., Venkatesan K., And Eapen K., "A Generalized Firing Angle Controller Using Phase-Locked Loop for Thyristor Control," *IEEE Transactions On Industrial Electronics And Control Instrumentation, IECI*-Feb 1981.

[6] T. C. Pimenta, L. L. G. Vermaas, P. C. Crepaldi, R. L. Moreno "The Design of a Digital IC for Thyristor Triggering,", *10th Intentional Conference on VLSI Design*–Jan 1997.

[7] E. Monmasson, and Y.A. Chapuis "Contributions of FPGAs to the Control of Electrical Systems, a Review" *IEEE Industrial Electronics Society Newsletter* ISSN 0746-1240 VOL. 49, NO. 4. 2002.

[8] Eric Monmasson and Marcian N cirstea "FPGA Design Methology for Industrial Control Systems- A Review", *IEEE Ttras.on Industrial Electronics vol-54*, no.-4, IEEE 2007.

[9] Czeslaw T. Kowalski, Jacek Lis, Teresa Orlowska-Kowalska: "FPGA Implementation of DTC Control Method for the Induction Motor Drive" , *The International Conference on "Computer as a Tool*" EUROCON 2007

[10] R.S.Dhekakar, N.V.Srikanth, M.Pravin Kumar,"Design, Modeling and Simulation of Fuzzy Controlled SVC for 750km (λ/8) transmission line" . *POWERCOIN- 08, International Conference 2008.*

[11] R.S.Dhekekar, N.V.Srikanth : "Implementation of Real time Fuzzy Control SVC", *International Journal of Electrical Engineering* Volume 10/edition 4, June 2010

[12] Narain G.Hingorani, "Understanding FACTS, Concepts and Technology of Flexible AC Transmission Systems", by *IEEE press USA.*

[13] Muhammad H. Rashid, Power Electronics (Circuits, Devices, and Applications), 3rd ed., *Pearson Prentice Hall,* 2006,

[14] SIM Power System User Guide MATLAB manual Version 4.

[15] J. Bhasker "VHDLPrimer' LPE low price edition

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