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Effectual SVPWM Techniques and Implementation of FPGA Based Induction Motor Drive

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ABSTRACT

This paper presents a field programmable gate array (FPGA)-based control integrated circuits (IC) for controlling the pulsewidth modulation (PWM) inverter used in power conditioning system for ac-voltage regulation. Space vector pulsewidth modulation (SVPWM) algorithm offers great flexibility to optimise switching waveform. Among them, double edge triggering can be implemented; It consumes less power compare to other PWM techniques. The SVPWM pulses thus generated through Xilinx is given as switching pulses to voltage source inverter (VSI) circuit to trigger the motor. The delay time of PWM output is programmable and SVPWM control IC is reprogrammable.It shows the advantage of lower total harmonic distortion (THD) without increasing the switching losses. Results are provided along with simulation analysis in terms of THD, output fundamental voltage and voltage transfer ratio to verify the feasibility of operation. The SVPWM switching pattern has been achieved with a fundamental frequency of 50Hz.

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1. INTRODUCTION

Because of advances in solid state power devices and microprocessors ,switching power converters are used in more and more modern motor drives to convert and deliver the required energy to the motor. Variable frequency ac drives are increasingly used for various applications in industry and traction. Pulse width modulated (PWM) dc-ac converters have a wide range of applications in ac motor drives and ac power conditioning systems [1]. The PWM strategy plays an important role in the minimization of harmonics and switching losses in these converters, especially in the three-phase applications.Various modulation strategies, control schemes, and realization techniques [2].

In the design of a PWM control IC, there are many factors need to be considered, such as simplicity, flexibility, and complexity in the circuit design. The width of the pulses changes from pulse to pulse according to a modulating signal. When a PWM signal is applied to the gate of a power transistor, it causes the tum on and turn off intervals of the transistor to change from one PWM period to another PWM period according to the same modulating signal.

As to modulation is concerned the space vector modulation (SVM) has attracted great interest in recent years. Because the harmonic better than those of the other modulation method. The advantage of lower THD is without increasing the switching losses. The emergence of multilevel inverters has been in increase since the last decade. These new types of converters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum.

Thus this paper demonstrates that a more efficient and faster solution is the use of Field Programmable Gate Array (FPGA's), it investigates how to generate a variable PWM waveform based on Xilinx FPGA and the proposed design is tested by functional/timing simulation and experiments.The rest of the paper is organized as follows. Section II pictorial representation of a three phase inverter circuit.Section III briefly introduces the principle of symmetrical space vector PWM method. Section IV details on FPGA.Section V the hardware circuit represented as an block diagram. Section VI explains the experimental results and Section VII is the conclusion.

2. MULTILEVEL AND THREE PHASE INVERTER CIRCUITS

Among the familiar topologies, the most popular one is cascaded multilevel inverter. It exhibits several attractive features such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches when compared to ordinary cascaded multilevel inverter [3].

The inverter consists of seven MOSFET switches and three separate DC sources with a load. By switching the MOSFETS at the appropriate firing angles, we can obtain the seven level output voltage. MOSFET is preferred because of its fast switching nature. Recent development in high switching frequency power devices, such as IGBT, offers the possibility of developing high frequency PWM control techniques.

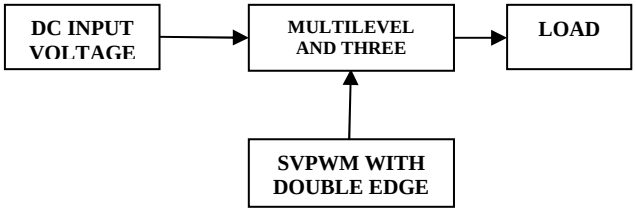

Figure 1. Block diagram of proposed FPGA based SVPWM control

3. PRINCIPLE OF SPACE VECTOR PWM

3.1 Principle of Pulse Width Modulation (PWM)

Fig. 2 shows circuit model of a single-phase inverter with a center-taped grounded DC bus,and Fig 3 illustrates principle of pulse width modulation.

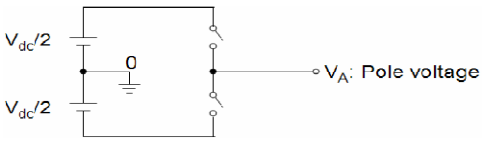

Figure 2. Circuit model of a single-phase inverter.

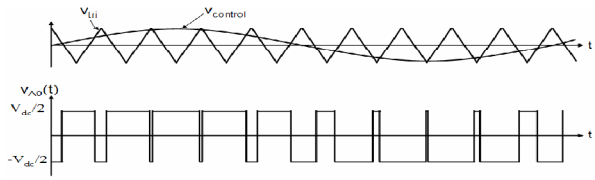

Figure 3. Pulse width modulation.

As depicted in Fig. 3, the inverter output voltage is determined in the following:

- When Vcontrol > Vtri, VA0 = Vdc/2
- When Vcontrol < Vtri, VA0 = −Vdc/2

Also, the inverter output voltage has the following features:

- PWM frequency is the same as the frequency of Vtri
- Amplitude is controlled by the peak value of Vcontrol
- Fundamental frequency is controlled by the frequency of Vcontrol

3.2 Principle of Space Vector PWM

The circuit model of a typical three-phase voltage source PWM inverter.S1 to S6 are the six power switches that shape the output, which are controlled by the switching variables a, a′, b, b′, c and c′. When an upper transistor is switched on, i.e., when a, b or c is 1. The corresponding lower transistor is switched off, i.e., the corresponding a′, b′ or c′ is 0.Therefore, The on and off states of the upper transistors S1, S3 and S5 can be used to determine the output voltage.

As illustrated in Fig. 4, there are eight possible combinations of on and off patterns for the three upper power switches. The on and off states of the lower power devices are opposite to the upper one and so are easily determined once the states of the upper power transistors are determined. the eight switching vectors, output line to neutral voltage (phase voltage), and output line-to-line voltages in terms of DC-link Vdc, are given in Table1 and Fig. 5 shows the eight inverter voltage vectors (V0 to V7).

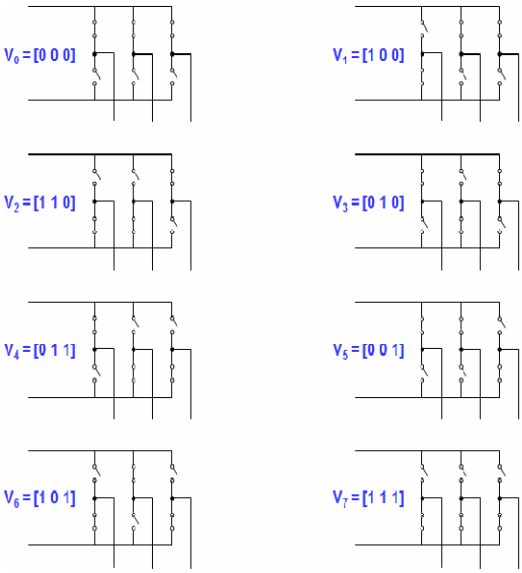

Figure 4. The eight inverter voltage vectors (V0 to V7).

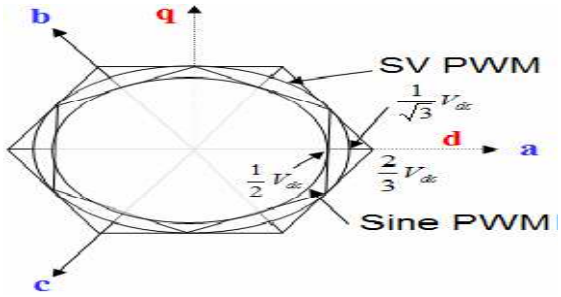

Figure 5. Locus comparison of maximum linear control voltage in Sine PWM and SVPWM.

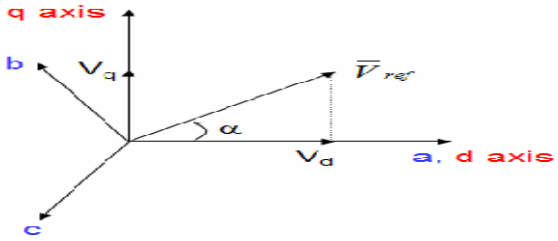

Figure 6. The relationship of abc reference frame and stationary dq reference frame.

Space Vector PWM (SVPWM) refers to a special switching sequence of the upper three power transistors of a three-phase power inverter. It has been shown to generate less harmonic distortion in the output voltages and or currents applied to the phases of an AC motor and to provide more efficient use of supply voltage compared with sinusoidal modulation technique as shown in Fig. 6.

$$\mathbf{f}dq0 = \mathbf{K}s\mathbf{f}abc$$

As described in Fig. 7, this transformation is equivalent to an orthogonal projection of [a, b,c]t onto the two-dimensional perpendicular to the vector [1, 1, 1]t (the equivalent d-q plane) in a three-dimensional coordinate system. As a result, six non-zero vectors and two zero vectors are possible. Six nonzero vectors (V1 - V6) shape the axes of a hexagonal as depicted in Fig. 8, and feed electric power to the load. The angle between any adjacent two non-zero vectors is 60 degrees. Meanwhile, two zero vectors (V0 and V7) are at the origin and apply zero voltage to the load. The eight vectors are called the basic space vectors and are denoted by V0, V1, V2, V3, V4,V5, V6, and V7. The same transformation can be applied to the desired output voltage to get the desired reference voltage vector Vref in the d-q plane.The objective of space vector PWM technique is to approximate the reference voltage vector Vref using the eight switching

patterns. One simple method of approximation is to generate the average output of the inverter in a small period, T to be the same as that of Vref in the same period.

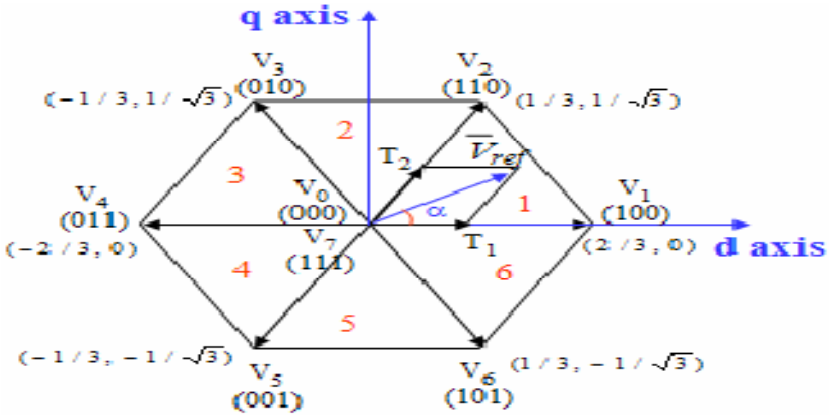

Figure 7. Basic switching vectors and sectors

Therefore, space vector PWM can be implemented by the following steps:
Step 1. Determine Vd, Vq, Vref, and angle (α)
Step 2. Determine time duration T1, T2, T0
Step 3. Determine the switching time of each transistor (S1 to S6)

3.2.1 Step 1: Determine Vd, Vq, Vref, and angle (α)

From Fig. 7, the Vd, Vq, Vref, and angle (α) can be determined as follows.

3.2.2 Step 2: Determine time duration T1, T2, T0

From Fig. 10, the switching time duration can be calculated as follows:

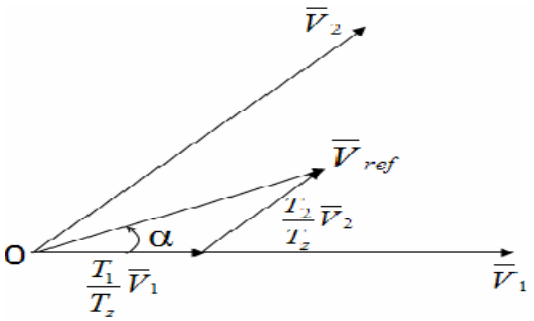

Figure 8.Reference vector as a combination of adjacent vectors at sector 1.

3.2.3 Step 3: Determine the switching time of each transistor (S1 to S6)

Simulation Steps:
(1) Initialize system parameters in MATLAB/SIMULNK .
(2) Perform M-File coding to
(i)Determine sector
(ii)Determine time duration T1, T2, T0
(iii)Determine the switching time (Ta, Tb, and Tc) of each transistor (S1 to S6)
(iv)Generate the inverter output voltages (VAB, VBC, VCA,)
(v)Generate VHDL Codings through software convertion tool
(vi)Burn the program in the FPGA kit
(vii) View the SVPWM waveforms through xilings.

4. FIELD PROGRAMMABLE GATE ARRAY

A Field-Programmable Gate Array or FPGA is a silicon chip containing an array of configurable logic blocks (CLBs). Unlike an Application Specific Integrated Circuit (ASIC) which can perform a single specific function for the lifetime of the chip an FPGA can be reprogrammed to perform different function in a matter of microseconds. The design used Xilinx development tools, namely Workview, and is realized in a single FPGA chip with no external memory[5]. The benefits of this design are as follows

The whole system is implemented in only a single chip consequently the circuit is very compact.

Systems of FPGA chip are more reliable because they do not need any control software

Faster design and verification time, design change without penalty.

In this paper programming FPGA using Hardware Description Languages and coding are used to generate the Space Vector Modulation for the inverter circuit. The point to be noted here is that instead of writing the direct VHDL Codings firstly the M-File codings are written to generate the SVPWM pulses and then after by using the software converter VHDL coding are generated.Therby the work requires less time and fast operation. The MATLAB/SIMULNK environment is familiar to vast number of software programmers and since m-file coding is very much common to most of the programmers it becomes easier for individuals to work in this software.

A very attractive high-level design/simulation tool is provided by FPGA and is called XILINX. It is a very flexible design tool, which allows Testing of a high-level structural description of the design and makes possible quick changes and corrections. The circuit description structure is very similar to the way the design could be implemented later. Therefore mapping tool allowing conversion of such a structure into VHDL code would save the designer's time, which otherwise has to be spent in rewriting the same structure in VHDL and probably making mistakes that will need debugging.

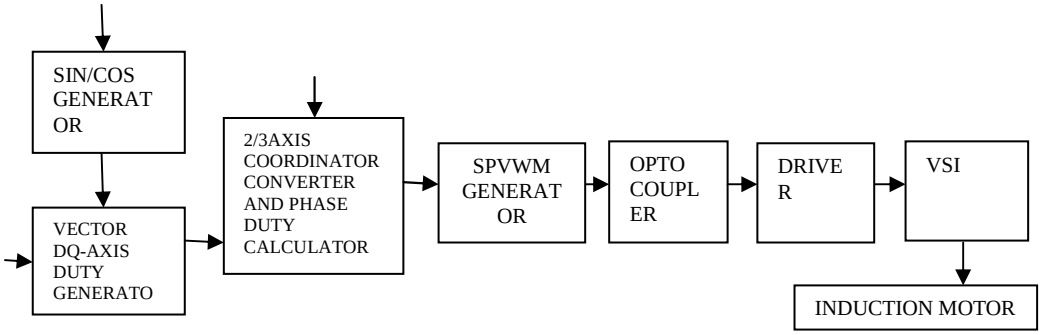

Figure 9. Diagram block of overall system

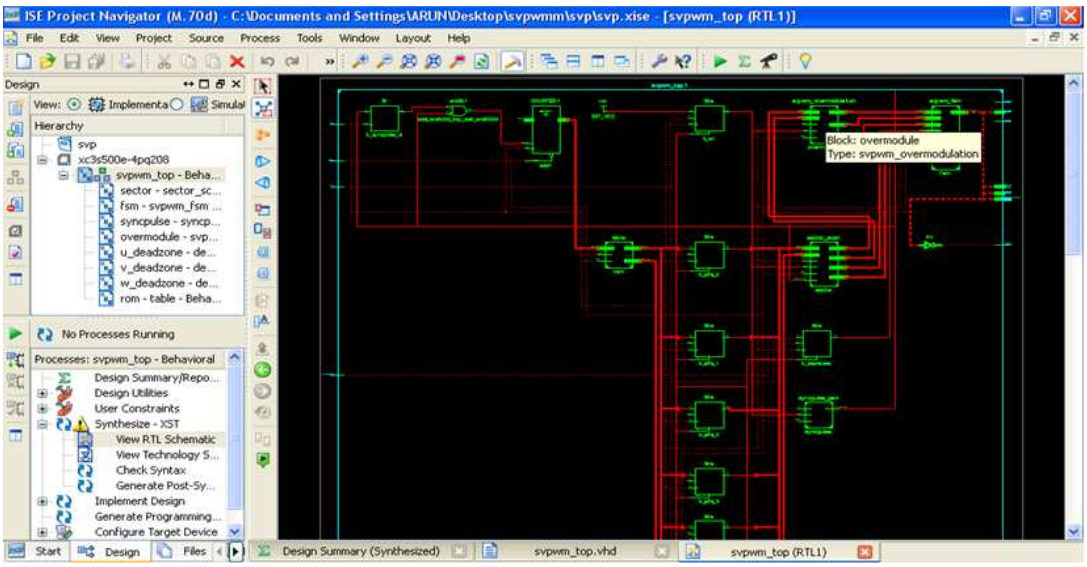

Figure 10. Expansion of each block in xilinx

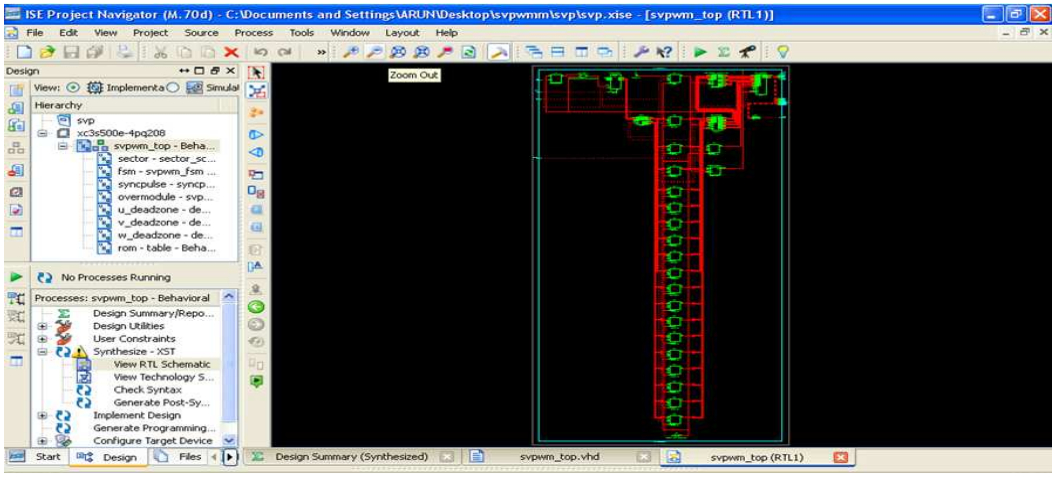

Figure 11. Shows schematic of the svpwm techniques in the Xilinx.

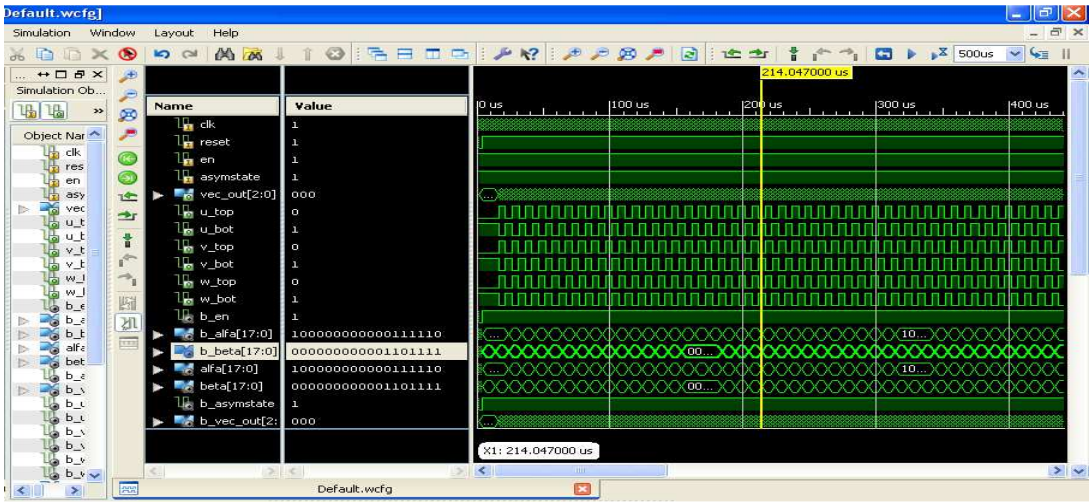

Figure 12. Shows the output waveform of SVPWM

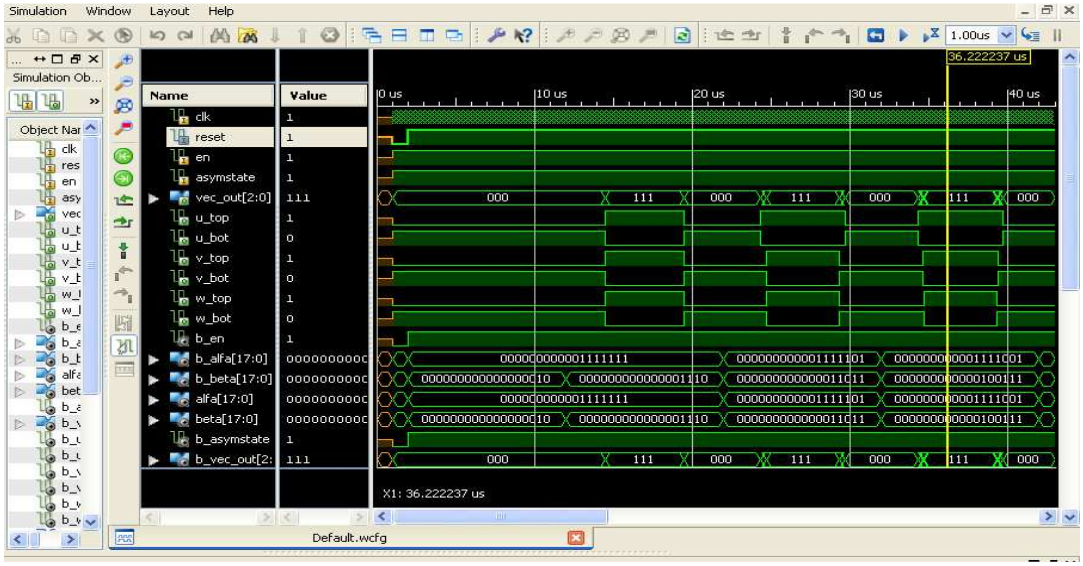

Figure 13. Shows the SVPWM techniques.

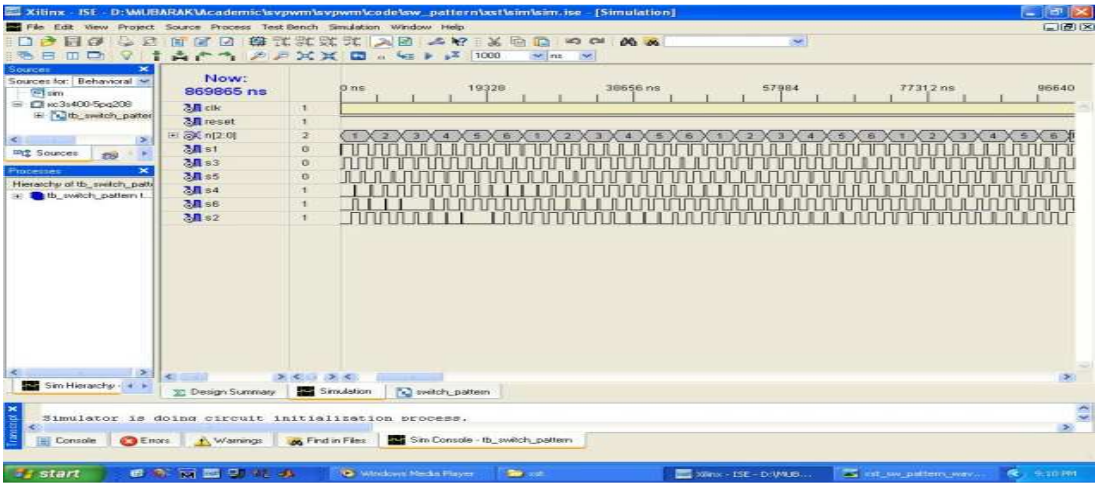

Figure 14. Introduce delay in the switches.

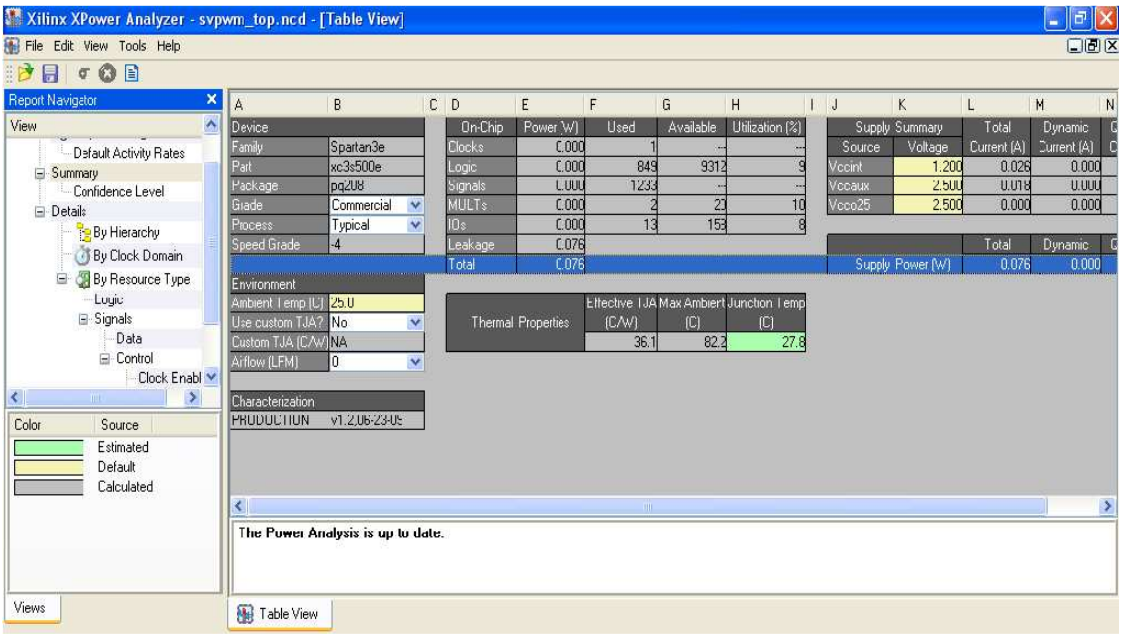

Figure 15. Table view

6. CONCLUSION

The designed Space Vector PWM control IC for induction motor drive has been simulated using single FPGA. The output fundamental frequency can be varied from 1.46 Hz to 1.5 kHz and the PWM switching frequency can be set from 195 Hz to 49.92 kHz. The delay time of PWM output is programmable. The designed SVPWM control IC is reprogrammable. The switching pattern generated will reduce the harmonic content,provides efficient as well flexible control and reduces the total size of the system. This SVPWM IC can be used for high performance ac drives and power conditioning equipment as a modulator.In this paper, a theoretical study concerning the SVPWM control strategy on the voltage inverter based on FPGA is presented. This aims on one hand to prove the effectiveness of the SVPWM in the contribution in the switching power losses reduction. SVPWM is among the best solution to achieve good voltage transfer and reduced harmonic distortion in the output of an inverter.

On the other hand since Field programmable gate array (FPGA) have better advantages compared to microprocessor and DSP control, this modulation technique is implemented in an FPGA by initially generating m-file through Matlab-Simulink environment. The FPGA coding makes it easier in designing the vector modulation pattern generator using field programmable Array .Moreover the MATLAB/SIMULNK environment is familiar to vast number of software programmers and since m-file

coding is very much common to most of the programmers it becomes easier for individuals to work in this software.

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