International Journal of Reconfigurable and Embedded Systems (IJRES)
Vol. 9, No. 1, March 2020, pp. 28~33
ISSN: 2089-4864, DOI: 10.11591/ijres.v9.i1.pp28-33

Low power 11T adder comparator design

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Article Info

Article history:

Received Apr 15, 2019
Revised Oct 10, 2019
Accepted Nov 11, 2019

Keywords:

1-bit adder comparator
Adder
Lower power
Speed
Top-down approach

ABSTRACT

Comparator is a basic arithmetic component in a digital system and adders are the basic block of processor unit, the performance of adder will improve the system performance. The proposed 11T adder comparator is consists of three main components, namely XOR, inverter, and MUX logic. The circuit is designed and implemented based on top-down approach with 11 transistors. The proposed cell can be used at higher temperature with minimal power loss. It also gives faster response for the carry output. The proposed comparator circuit shows 63.80% improvement in power consumption than other circuits.

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1. INTRODUCTION

The comparator is one of the vital components of digital systems. The CMOS comparators are designed with different power dissipation, delay and circuit complexity. The implementation of full adder in comparator has been constantly improving since it first design. The adder as a design, mainly to reduce the number of transistors, minimize the power consumption and increase the speed. It has been used in many electronic devices and wireless sensor networks (WSN). Most of the researchers have designed the comparator circuit and improved the performance in aspect of sensitivity, offset, speed and power dissipation by using different type of topologies and circuit methods [1-2].

Magnitude comparator is used in digital system to compare two inputs (A and B) and relative magnitude to find three states of outcome whether A is less than B, A is equal to B or A is greater than B. The main focus is to use full adder for low magnitude comparator. The magnitude comparator with full adder inputs (A and B), inverts the input A and AND gates result as output. The three outputs are obtained by different combination of inputs. CMOS Comparator is designed with various logic styles into an integrated design methodology. A CMOS Comparator design, both quantitative and qualitative has been individually investigated and analyzed. Clocked regeneration comparators are called as dynamic comparators. Normally, these comparators are used in many applications with Analog to Digital Converters and need quick decision and positive feedback in the regeneration circuits. Many designs are analyzed in in terms of noise, offset, random decision errors, speed and kick–back noise [3-7]. Due to the disadvantages of dynamic comparator, a study of double–tail comparator is been proposed [8]. The comparator operates at lower supply voltages due to less stacking effect. It is also suitable for quick latching and independent of the input common mode voltage as well as a small current in the input stage for low offset. Generally, the three major concerns of

CMOS comparator design are power consumption, speed and chip area. Hence these estimates create conflict with others. Each individual concern cannot be optimized independently [9]. The GDI and PTL logics were used for One bit hybrid comparator consisting of 17T (8 PMOS and 9 NMOS). The basic building block (9T Full adder) is implemented in PTL and GDI logic. The hybrid logic used results in additional propagation delay along with switching penalty. Moreover, the increased complexity and overall performance degradation are caused.

This paper is arranged as follows. The section 2 explains the proposed design with layout and generated waveforms. Section 3 includes the results analysis and discussion. The paper ends with conclusion and references.

2. PROPOSED DESIGN

The proposed comparator design has an adder circuit with 11 transistors as shown in Figure 1 and Figure 2. Due to minimum number of transistors, the comparator circuit consumes less power. It consists of three main components, namely XOR, inverter, and MUX logic. The (one bit) output Boolean expression for SUM and CARRY of adder are shown below:

$$SUM = \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C} + A\overline{BC}$$

$$CARRY = AB + AC + BC$$

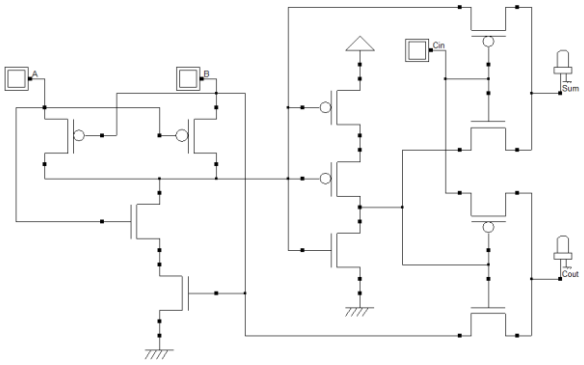

Figure 1. Adder design of 11T adder

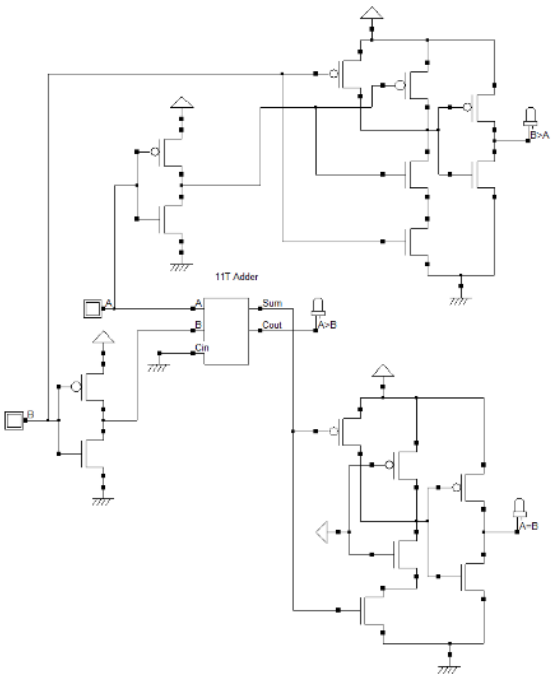

Figure 2. 11T adder comparator

The three comparative outputs are obtained by connecting the inputs A and B to the full adder and the input C is grounded. When A>B, the comparator output acts as the carry output (1-bit). The AND gate input combinations are used for the combinations of A=B and B>A. When B>A, the AND gate input combinations are B and Abar and for A=B, it is SUM and $V_{DD.}$

3. RESULT AND DISCUSSION

The proposed 11T adder comparator is designed using three main components (XOR, inverter, and MUX logic), other comparator (1 bit) circuits (6T, 14T, 7T, 12T) and Shannon are simulated using Microwind CAD tool. Figure 3 shows the layout of comparator which is simulated at 65nm CMOS technology by using BSIM 4 VLSI CAD tool. The proposed 11T adder comparator circuit provides fast, minimum power and less area when compared to the four adder cell based comparator circuits. The reasons are as follows: The Shannon comparator circuit dissipates large power and more delay due to the voltage swing restoration problem in their adder component [10].

In the MUX-14T adder cell, the input node dissipates more power to transmit the voltage level [11]. Due to the input nodes transients, the MCIT-7T adder cell based circuit consumes high power [12]. The large power consumption and low speed are the main drawbacks of the MUX-12T design [13]. It is due to buffering restoration unit at A⊕B in the carry circuit.

The proposed 11T comparator circuit is compared with 120, 90 and 45 nm feature sizes of other comparators exist in the literature. Figure 3 shows the generated layout of 11T adder comparator. The waveform of the 11T comparator is shown in Figure 4. Due to high current, minimum number of transistors, more transitions in NMOS, absence of swing restoration, and minimum critical path in comparator circuit, the proposed 11T comparator performance is improved. Table 1 shows the transient analog simulation.

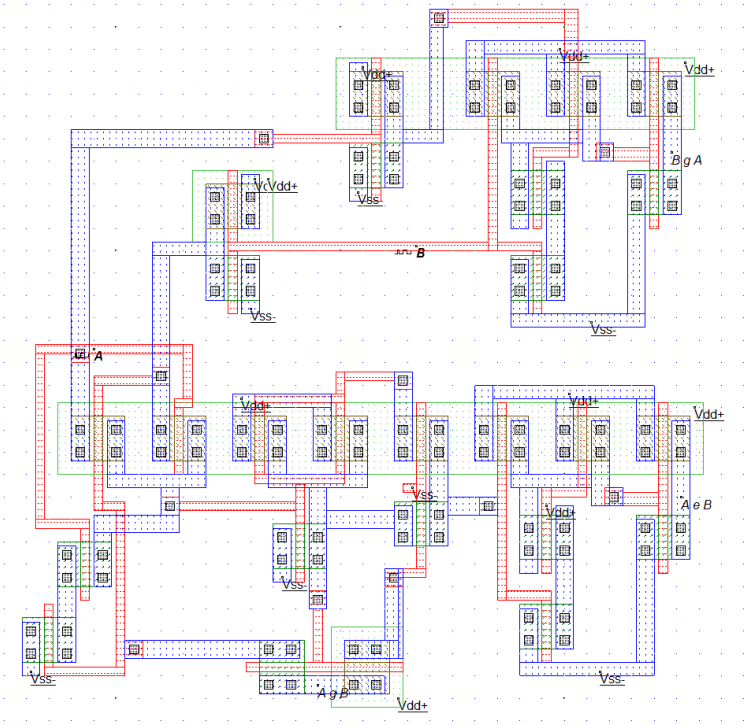

Figure 3. Layout diagram of 11T adder comparator

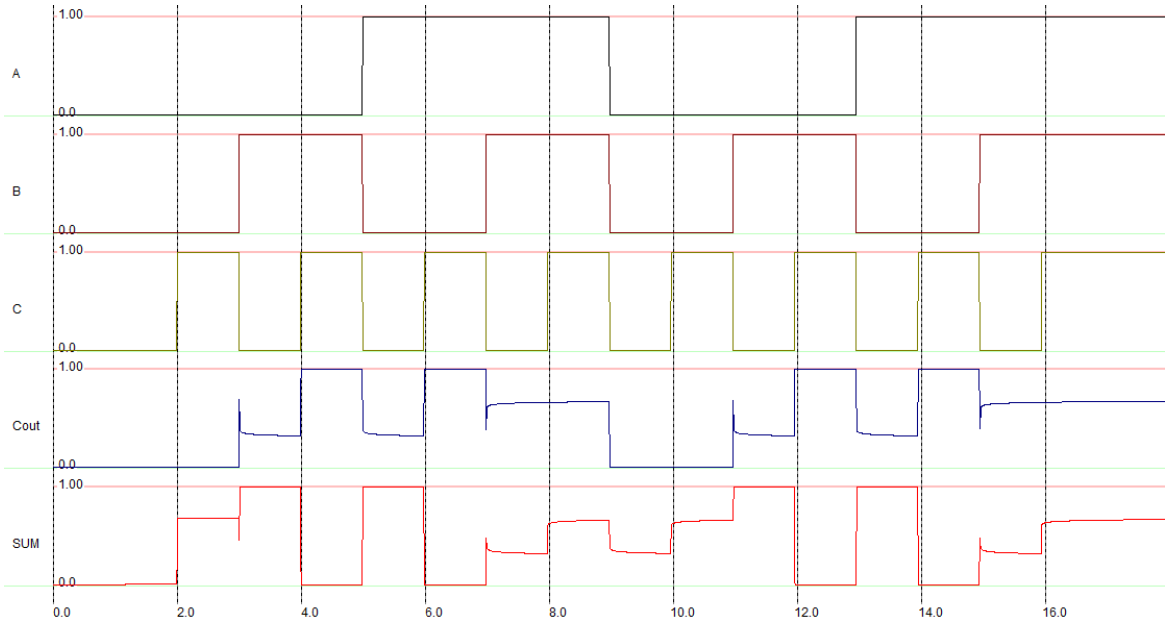

Figure 4. Generated wave forms of 11T adder comparator

Table 1. The transient analog simulation

Circuit	Power supply	65nm	90nm	130nm	180nm
11T adder comparator	Power (µW)	18.810	56.084	43.056	93.173
	Delay (ps)	6	8	7	17
	Area (μm^2)	24×6	30×7	41×10	83×21
1-bit comparator (MUX 6T) [14]	Power (µW)	29.46	34.36	75.82	97.68
	Delay (ps)	6	8	9	12
	Area (μm^2)	22×7	23×10	30×10	68×21
1-bit comparator (MUX 12T) [14]	Power (µW)	46.33	51.33	84.87	130.33
	Delay (ps)	7	7	10	14
	Area (μm^2)	29×7	32×12	45×11	74×51
1-bit comparator (MUX 14T) [14]	Power (µW)	46.55	98.5	119.06	182.22
	Delay (ps)	15	17	24	32
	Area (μm^2)	29×9	38×12	54×11	114×24
1-bit comparator (MCIT 7T) [14]	Power (µW)	42.23	51.66	78.11	139.82
	Delay (ps)	15	16	21	26
	Area (μm^2)	25×8	29×10	50×10	79×55
1-bit comparator (Shannon) [14]	Power (µW)	112.27	250.6	428.26	720.56
	Delay (ps)	15	19	24	35
	Area (μm^2)	47×7	54×11	60×13	124×23

3.1. Power dissipation

The power dissipation can be assign to two categories in the digital circuit design. The dynamic dissipation and also the static dissipation. Dynamic dissipation is caused due to the switching activity causes the transient current produce, when the switch is charged and discharge, the parasitic capacitance will be also affected. And for the static dissipation, it is caused by the leakage current drawn by the supply power. The static power is nothing but the product of supply voltage and leakage current. Power consumption is moderately high at 11T adder comparator cause of increase dynamic power by NMOS circuit design. Switching activity of the transistor will cause the high power consumption and it can be estimated by the vectors using the MICROWIND simulator.

3.2. Propagation delay

When the input signal of logic gate is changed, propagation delay from changes output of the logic gate occur due the load capacitance effect at output node. The 11T adder circuit is designed as high-speed circuit in latest trend.

The propagation delay of the proposed 11T adder comparator is evaluated by simulation considering increment of the capacitance as shown in Figure 5. The delay response of three different conditions, high speed (HS), high voltage (HV) and low power (LP) are described in Figure 6. The high

speed PMOS and NMOS cells design gives good propagation delay compared to other cells FETs. Although the circuit is complex, the derived (1) depicts its dependency of the comparator parameters. The HS FET cells' W/L ratio is less compared to the LP FET and HV cells gives high speed.

$$T_d = \frac{C_L V_{DD}}{I} = \frac{C_L V_{DD}}{\eta(W/L)(V_{DD} - V_{th})^2} \quad (1)$$

T_d is defined as propagation delay of the comparator, W/L is the length/width ration of the transistor and Vt_h is threshold voltage. Due to reduced switching activity in 11T Adder based comparator, the propagation delay is minimized and it is widely used in high speed mobile communication.

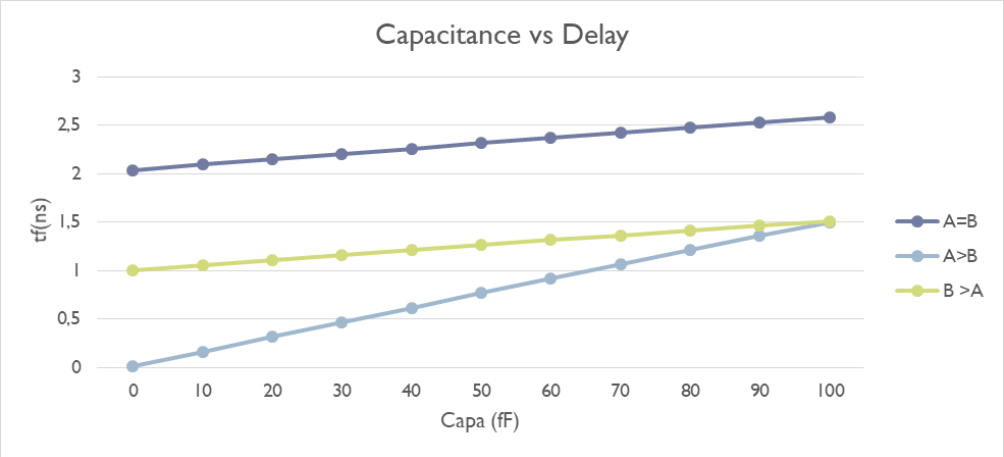

Figure 5. Capacitance vs delay of 11T adder comparator

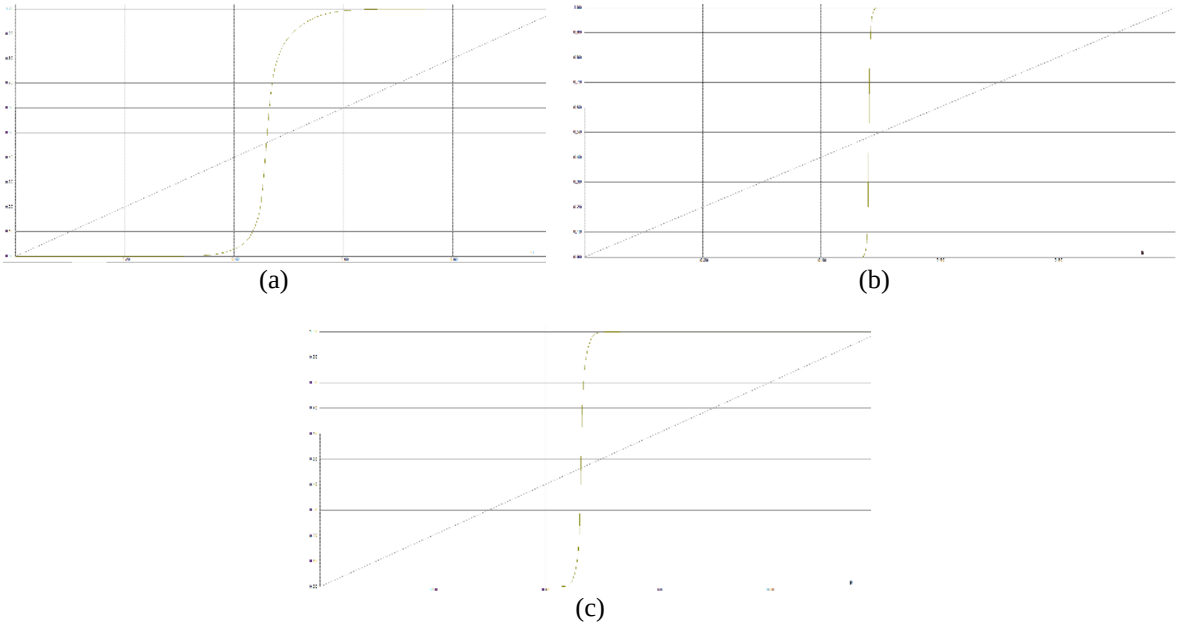

Figure 6. Static characteristics of the 11T adder comparator; a) High speed (HS), b) High voltage (HV), c) Low voltage (LV)

4. CONCLUSION

An 11T adder comparator (1-bit) has been introduced. The 11T comparator has been analyzed with different circuits to highlight that the good design in the aspect of power consumption. It is designed with DSCH 3.5. Microwind 3.5 CAD tool is used to generate layouts. The 11T comparator is compared with existing designs at 180,120, 90 and 65nm features sizes. Analysis done by using BSIM 4 tools and static characteristics also analyzed. Further, the 11T adder comparator (1 bit) is compared with five existing adder in terms of power, capacitance with speed and area. The results proved that the 11T comparator circuit is much better than the existing circuits. The 11T adder comparator is suitable to adopt with low power and high speed mobile communication application.

REFERENCES

[1] B. Goll and H. Zimmermann, "A 0.12 μm CMOS comparator requiring 0.5V at 600MHz and 1.5V at 6 GHz," *in Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, pp. 316–317, Feb. 2007.

[2] B. Goll and H. Zimmermann, "Low-power 600MHz comparator for 0.5 V supply voltage in 0.12 μm CMOS," *IEEE Electron. Letter*, vol. 43, no. 7, pp. 388–390, Mar. 2007.

[3] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. Vander Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.

[4] S. Babayan-Mashhadi and R. Lotfi, "An offset cancellation technique for comparators using body-voltage trimming," *Int. J. Analog Integr. Circuits Signal Process.*, vol. 73, no. 3, pp. 673–682, Dec. 2012.

[5] J. He, S. Zhan, D. Chen, and R. J. Geiger, "Analyses of static and dynamic random offset voltages in dynamic comparators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 911–919, May 2009.

[6] J. Kim, B. S. Leibowits, J. Ren, and C. J. Madden, "Simulation and analysis of random decision errors in clocked comparators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1844–1857, Aug. 2009.

[7] P. M. Figueiredo and J. C. Vital, "Kickback noise reduction technique for CMOS latched comapartors," *IEEE Trans. Circuits Syst. II, Exp.Briefs*, vol. 53, no. 7, pp. 541–545, Jul. 2006.

[8] D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps Setup/Hold time," *in Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, pp. 314–315, Feb. 2007.

[9] Anjali, S., S. Richa and P. Kajla, "Area efficient 1-bit comparator design by using hybridized full adder module based on PTL and GDI logic," *Int. J. Comput. Applic*., vol. 82, pp. 5-13, 2013.

[10] Senthilpari, C., K. Diwakar and A.K. Singh, "Low energy, low latency and high speed array divider circuit using a Shannon theorem based adder cell," *J. Recent Patents Nanotechnology*, vol. 3, pp. 61-72, 2009.

[11] Senthilpari, C., S. Kavitha and J. Joseph, "Lower delay and area efficient non-restoring array divider by using Shannon based adder technique," *Proceedings of IEEE International Conference on Semiconductor Electronics, Jun. 28-30, IEEE Xplore Press*, pp. 140-144, 2010.

[12] Senthilpari, C., I.M. Zuraida and S. Kavitha, "Proposed low power, high speed adder-based 65 nm square root circuit," *Microelectron J.*, vol. 42, pp. 445-451, 2011.

[13] G. Ramana Murthy, Ajay Kumar Singh, P. Velraj Kumar and Tan Wee Xin Wilson, "Design of a Low Power and High Speed Comparator using MUX based Full Adder Cell for Mobile Communications," *American Journal of Applied Sciences*, vol. 14, no. 1, pp. 116-123, 2017.

[14] Ramana Murthy, G., C. Senthilpari, P. Velrajkumar and T.S. Lim, "Leakage current optimization for novel MUX-Based full-adder cell in CMOS 130nm technology," *Proceedings of the Conference on TENCON, (CON' 11)*, IEEE, pp. 734-738, 2011.