

Design and Analysis of CMOS Low Noise Amplifier Circuit for 5-ghz Cascode and Folded Cascode in 180nm Technology

T. Kanthi, D.Sharath Babu Rao

Department of ECE., G.P.R.E.C, Kurnool, India

Article Info

Article history:

Received Agu 5, 2018

Revised Oct 6, 2018

Accepted Oct 19, 2018

Keywords:

Low noise amplifiers

Noise figure

Power gain

ABSTRACT

This paper is about Low noise amplifier topologies based on 0.18 μ m CMOS technology. A common source stage with inductive degeneration, cascode stage and folded cascode stage is designed, simulated and the performance has been analyzed. The LNA's are designed in 5GHz. The LNA of cascode stage of noise figure (NF) 2.044dB and power gain 4.347 is achieved. The simulations are done in cadence virtuoso spectre RF.

Copyright © 2018 nstitute of Advanced Engineering and Science.
All rights reserved.

Corresponding Author:

T. Kanthi,
Department of ECE., G.P.R.E.C, Kurnool, India
Email: thiruveedulakanthi@gmail.com

1. INTRODUCTION

Due to rapid growth of wireless communication industry, the increasing demand upon wireless devices has motivated the development of CMOS radio frequency integrated circuits (RFICs). LNAs are used in various wireless applications like Wi-Fi, Bluetooth, wireless voice, data and video. Many of this applications operate in 2 to 5GHz. The Wi-Fi of IEEE 802.11ac protocol is used for 5GHz band.

1.1. RF Design

Many decades of work on RF and Microwave theory and two decades of research on RF IC's. Design and implementation of RF circuit and transceiver remains challenging. RF circuits and transceiver must deal with numerous trade-offs. The demand for high performance, lower cost and greater functionality continues to present new challenges. RF design hexagon, consists of six parameters related with each other to some extent. RF design of parameters is represented in a Figure 1.

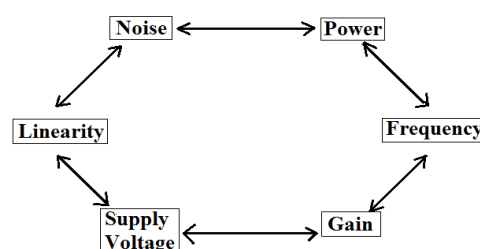


Figure 1. Rf design hexagon

Low Noise amplifiers are based on Radio frequency communication receivers and the specifications we can estimate overall noise performance of the RF receivers. The RF signal received at the antenna is weak, using an amplifier with high gain and noise performance is needed to amplify the signal before it can be fed to other parts of the receiver. Such amplifier is referred to as a Low Noise Amplifier (LNA).

1.2. Low Noise Amplifier

The Low noise amplifiers are one of the basic building blocks of any communication systems. The demand of high performance wireless front-end system is increasing nowadays. The main aim on low power mobile devices with low cost. Low noise amplifier is the first stage of an RF receiver contributes to the noise of the entire receiver. The main function of the LNA is to amplify the weak signals from the antenna.

The first stage of the receiver contributes mainly to the overall Noise Figure (NF) of the receiver. The main performance parameters of LNAs are Gain, Noise Figure (NF), linearity and stability. The forward gain of LNA is defined by the S-parameters. The NF is defined as the ratio of signal to Noise Ratio (SNR) at the input to the SNR at the output. Third-order intercept point (IP₃) and 1dB compression point (P1dB) are the measures of linearity. LNA is stable it satisfies the condition stability Factor, $K > 1$. But always there will be a trade-offs in power, linearity, gain frequency and noise and of the design parameters.

The design and simulation of basic Common Source (CS) stage with inductive degeneration, using Cascode stage and Folded Cascode stage. The designed cascode stage is having a NF which is very less compared to the LNAs. The cascode LNA can used in an environment with weak signal strength as it is having a very good gain. Section II deals with the basic concepts of different methods of LNA topologies. Section III having the design considerations. In section IV reported about simulation results and in section V reported the conclusion.

2. BASIC LOW NOISE AMPLIFIER TOPOLOGIES

LNA topologies using Common Source and Common Drain with Cascode and Folded Cascode.

2.1. Common Source (CS) with Inductive Degeneration

The inductive degenerated topology is narrow-band since the input matching circuit consisting of the source inductors and the gate to source capacitance, C_{gs} , resonates at a single frequency. The inductively degenerated LNA is the dominating topology for narrow-band systems due to its advantages such as low Noise Figure of input matching, high gain, and low-power consumption. Common Source LNA forms a series RLC network as shown in Figure 2. The input impedance of the stage is given by the equation is

$$Z_{in} = S(L_S + L_g) + \frac{1}{sC_{gs}} + \left(\frac{gm_1}{C_{gs}}\right)L_S$$

$$Z_{in} \approx \omega_T L_S \text{ (at resonance)}$$

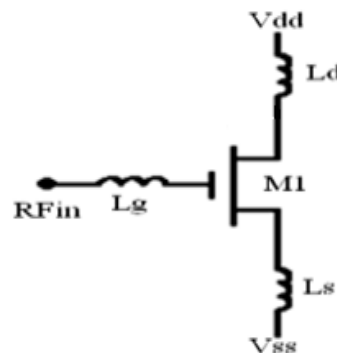


Figure 2. Common source of inductive degeneration

2.2. Cascode

The most commonly used topology for LNA design is the cascode amplifier with inductive source degeneration. The cascode topology has higher gain, due to the increase in the output impedance.

The cascode transistor suppresses the Miller capacitance of the reverse isolation. The suppression of the parasitic capacitance of the input transistor is suppressed which improves the high frequency operation of the amplifier. Figure 3 shown single ended cascode low noise amplifier.

2.3. Folded Cascode

In a cascode stage, relatively large bias voltage is required due to the stacking design of the Common Source and Common gate transistors. So for Low voltage applications, a folded cascode topology is used. Due to absence of stacking gain stages, the operating voltage of the folded cascode LNA can be reduced by one transistor overdrive. The advantages of the cascode stage are good linearity, Noise Figure, and bias stability. But the low gain is the one of the disadvantages of the folded cascode topology refer Figure 4.

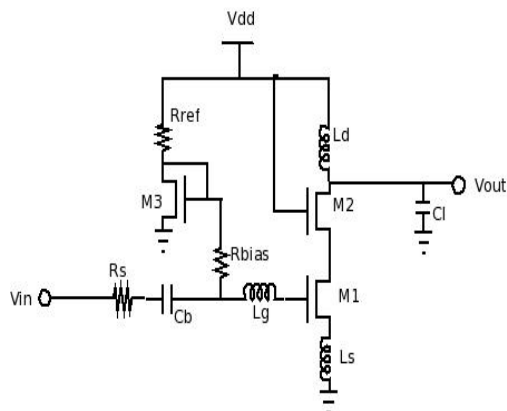


Figure 3. Single ended cascode low noise amplifier

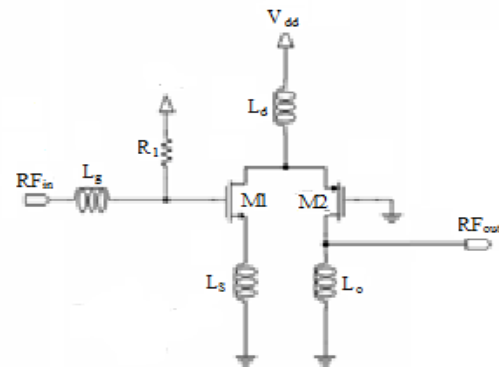


Figure 4. Folded cascode

3. DESIGNING

Using various applications in the 5GHz have varying design constraints. For the gain and Noise Figure should be extremely 40dB and 1dB respectively. Design Sepcifications as shown in Table 1.

Table 1. Design Sepcifications

Parameter	Value
Frequency	5ghz
Technology	180nm
Noise figure (db)	2.044db
Gain (db)	-36.754db
Supply voltage	1.8v
Power consumption (mw)	35.573db
Third order intercept point (dbm)	3dbm

The equations from equation (1) to equation (9) are used to design the source inductor L_s , gate inductor L_g , drain inductor L_d and width of the input device W .

$$W = \frac{1}{3W_0 L_{eff} C_{ox} R_s} \quad (1)$$

$$\omega_0 = 2\pi f_T \quad (2)$$

$$C_{gs1} = \frac{2}{3} W_{m1} L_{eff} C_{ox} \quad (3)$$

$$g_{m1} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) m1 ID1} \quad (4)$$

$$T = \frac{gm1}{C_{gs1}} \quad (5)$$

$$R_S = \frac{gm1 L_s}{C_{gs1}} \cong \omega_T L_s \quad (6)$$

$$L_s = \frac{R_s}{\omega_T} \quad (7)$$

$$L_g = \frac{1}{\omega_o^2 C_{gs1}} L_s \quad (8)$$

$$L_d = \frac{1}{\omega_o^2 C_L} \quad (9)$$

Where g_m is the trans-conductance of the device, C_{gs} is the gate source capacitance and R_s is the source resistance which is equal to 50Ω in equation (6) and in equation (7) is the unity gain frequency of the MOS transistor. ω_o is the centre frequency which is chosen to be 5GHz. In equation (1) C_{ox} is the oxide capacitance and L_{min} is the minimum channel length which is $0.18\mu m$ in this design.

4. SIMULATION RESULTS

4.1. Cascode-LNA

The Cascode LNA consists of three NMOS transistors are placed, transistor M1 is common source and M2 is common gate are connected to the inductive degeneration of L_s , L_d , L_g and connected to LC tank. S-parameters of two ports are connected to the input and output of LNA. Cascode LNA is used further reduce the power consumption and improve the NF and Gain. The aspect ratio of the input device of width and length of transistor M1 and M2 and is $140\mu m/180nm$ and M3 is $28\mu m/180nm$. Where L_g is $7nH$, L_s is $1.72nH$, L_d is $0.25nH$. Capacitance C_o and $C1$ is $10nH$ and $C2$ is $500fF$. Resistance R_{ref} is $2K\Omega$, R_{bias} is $3K\Omega$ and $R2$ is 300Ω . The cascode LNA of Noise Figure (NF) $3.250dB$ and power gain is $-41.355dB$, IIP3 is -4.722 . Cascode-LNA as shown in Figures 5-13.

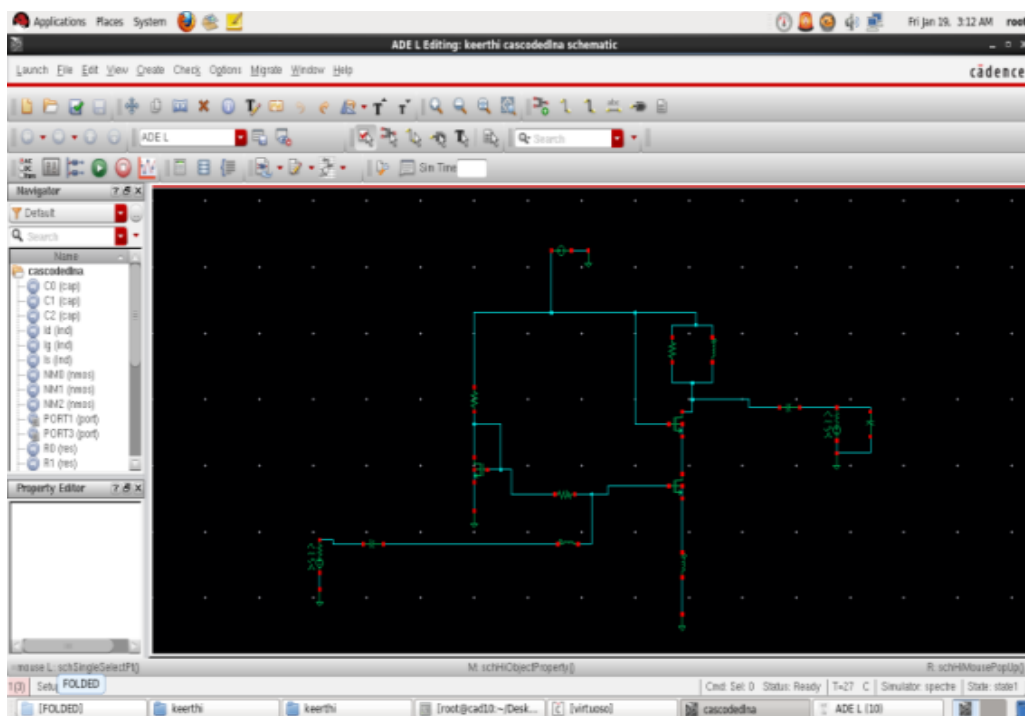


Figure 5. Schematic design of cascode low noise amplifier

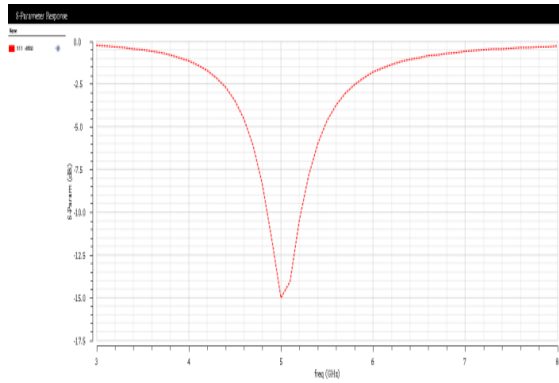


Figure 6. S11 of cascode low noise amplifier

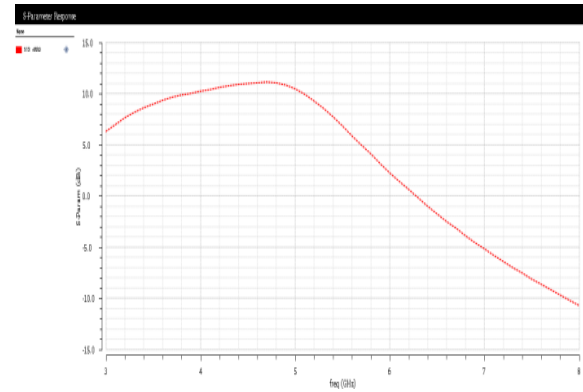


Figure 7. S12 of cascode low noise amplifier

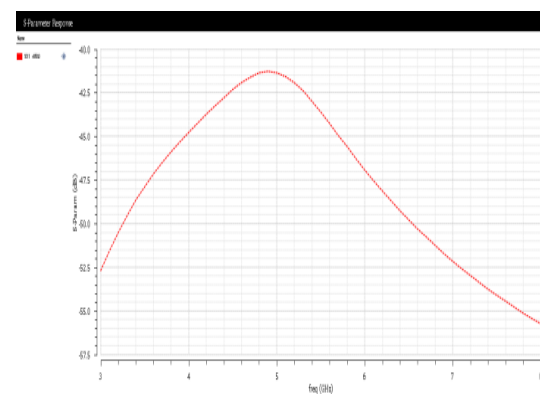


Figure 8. S21 of cascode low noise amplifier

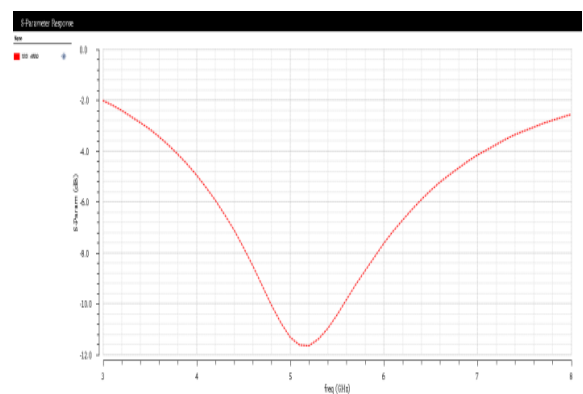


Figure 9. S22 of cascode low noise amplifier

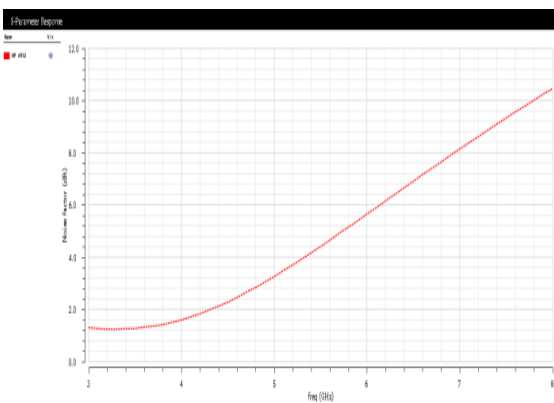


Figure 10. Noise figure of cascode low noise amplifier

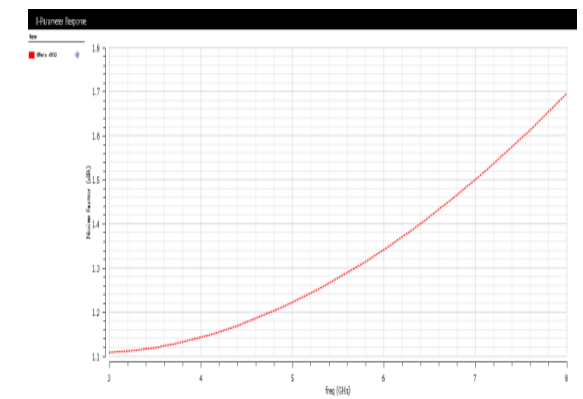


Figure 11. Minimum noise figure of cascode low noise amplifier

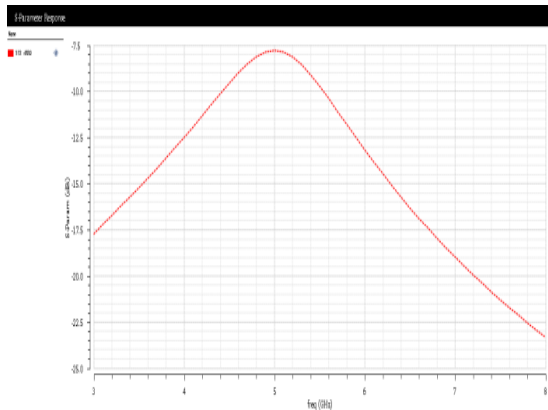


Figure 12. of Folded Cascode Low Noise Amplifier

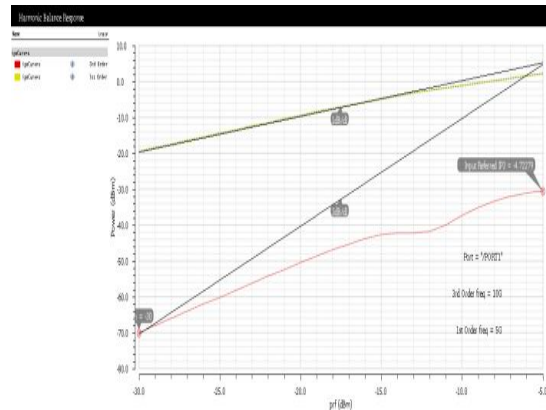


Figure 13. IPN Curves of Cascode Low Noise Amplifier

4.2. Folded Cascode LNA

The folded cascode topology is designed to further improve the NF. In folded cascode LNA common source is NMOS is M1 transistor and common gate is PMOS is M2 transistor having the same aspect ratio. The circuit design using RC network is added in parallel with the inductor, L_d is 1.5nH, L_g is 5.7nH, L_s is 0.25nH, L_o is 6nH, capacitance C_o and C_1 is 10nF, C_2 is 500fF, Port1 is 50 Ω and Port2 is 500 Ω . Transistors M1 is 140 μ m/180nm and M2 is 560 μ m/180nm. Resistance R_o is 300 Ω . Folded Cascode LNA as shown in Figures 14-20. Performance specifications between Cascode LNA and Folded Cascode LNA as shown in Table 2.

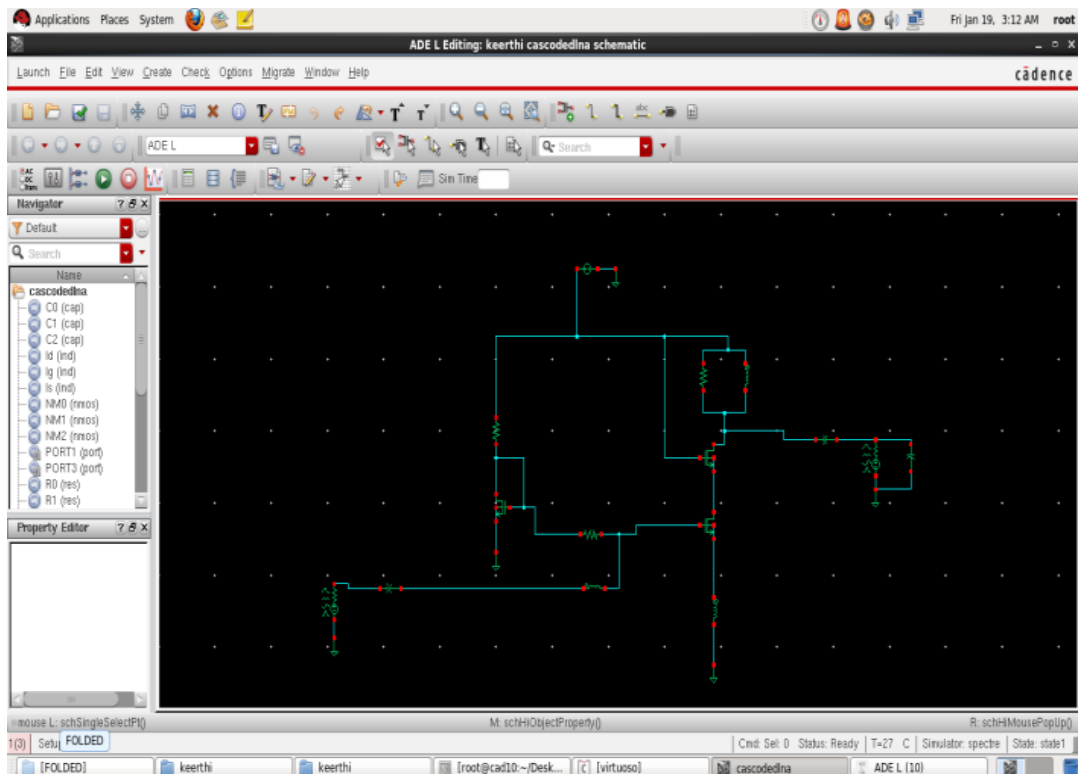


Figure 14. Schematic design of folded cascode low noise amplifier

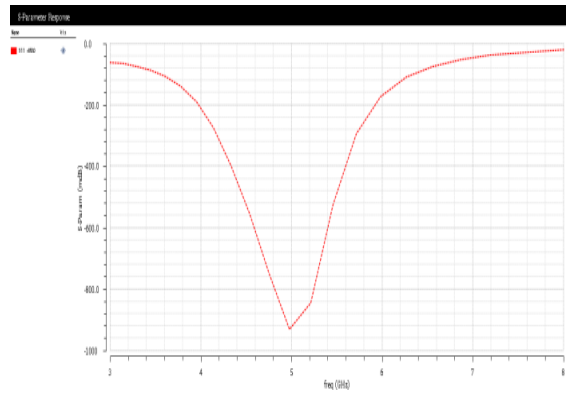


Figure 15. S11 of folded cascode low noise amplifier

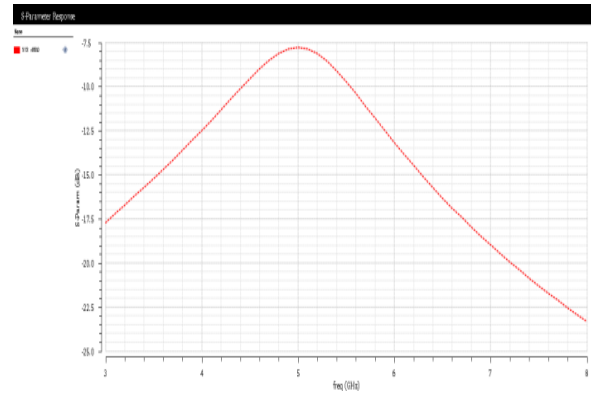


Figure 16. S12 of folded cascode low noise amplifier

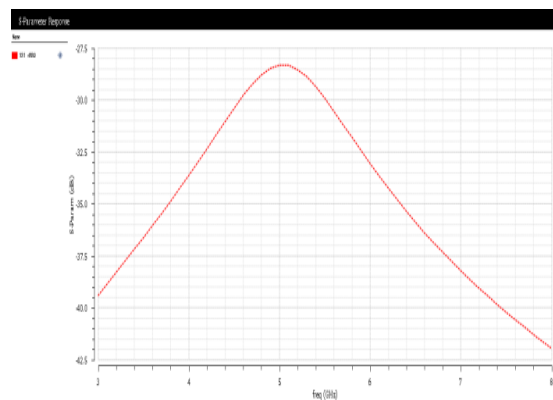


Figure 17. S21 of folded cascode low noise amplifier

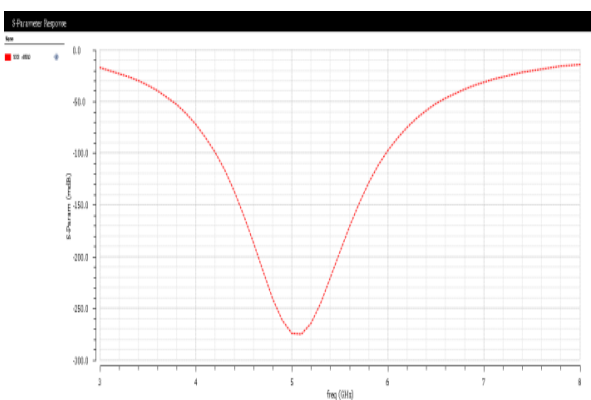


Figure 18. S22 of folded cascode low noise amplifier

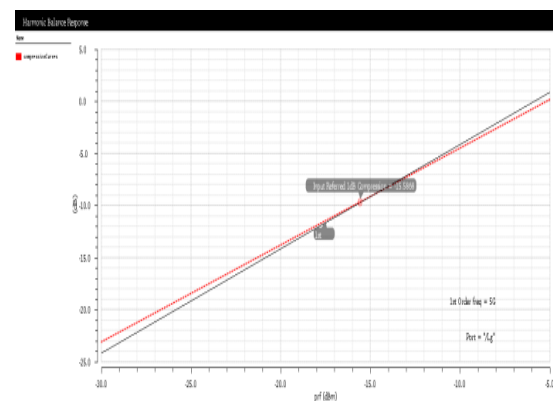


Figure 19. 1dB-compression of folded cascode low noise amplifier

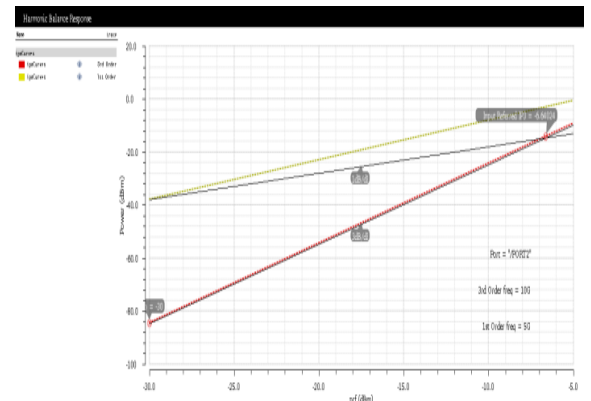


Figure 20. IPN curves of folded cascode low noise amplifier

Table 2. Performance Specifications

	Cascode LNA	Folded Cascode LNA
Frequency	5GHz	5GHz
Technology	180nm	180nm
Supply Voltage	1.8 V	1.8 V
S11 (dB)	-12.44dB	-10.17dB
S12 (dB)	10.436dB	3.98dB
S21 (dB)	-41.355dB	-22.81dB
S22 (dB)	-11.33dB	-5.38dB
NF (dB)	3.2509dB	2.64dB
NF _{min}	1.2215dB	1.715dB
1dB-compression	-12.0304	-15.5868
IIP3	-4.722	-6.640
Power	-49.573dB	-67.789dB

5. CONCLUSION

The design of 5GHz CMOS Cascode and Folded Cascode Low Noise Amplifier of Source Inductive Degeneration circuit of RF design of hexagon of Cascode Low Noise Amplifier of Noise Figure (NF) is 3.25dB and Gain is -41.35dB, Power Gain is -11.120, 1dB-compression point is -12.03 and IIP3 is -4.722 and Folded Cascode Low Noise Amplifier of Noise Figure is 2.64dB, Gain is -22.81dB, 1dB-compression point is -15.586 and IIP3 is -6.640 is demonstrated in this paper

REFERENCES

- [1] B. Razavi, RF Microelectronics, second edition ed. Prentice Hall, 2011.
- [2] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," IEEE J. Solid-State Circuits, vol.32, no.5, pp. 745-759, May 1997.
- [3] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise cancelling," IEEE J. Solid-State Circuits, vol.39, no. 2, pp.275-282, Feb. 2004.
- [4] Lorenzo, Michael Angelo G., and Maria Theresa G. De Leon. "Comparison of LNA topologies for WiMAX applications in a standard 90-nm CMOS process." In Computer Modelling and Simulation (UKSim), 2010 12th International Conference on, pp. 642-647. IEEE, 2010.
- [5] Hsieh, H-H., J-H. Wang, and L-H. Lu. "Gain-enhancement techniques for CMOS folded cascode LNAs at low-voltage operations." Microwave Theory and Techniques, IEEE Transactions on 56.8 (2008): 1807-1816.
- [6] T. Lee, The design of CMOS Radio Frequency Circuits, second edition ed. Prentice Hall, 2003.
- [7] B. J Sanghoon Joo, Tae-Young Choi, "A 2.4-GHz Resistive Feedback LNA in 0.13 μ m CMOS," IEEE journal of solid-state circuits, vol. 44, November 2009.
- [8] Kim, C. W., M. S Kang, P. T. Anh, and S. G. Lee, "An ultra wide band CMOS low noise amplifier for 3-5 GHz UWB system," IEEE journal of solid state circuits, vol. 40, no. 2, pp.544-547, Feb. 2005.
- [9] A. Bevilacqua, C. Sandner, A. Gerosa, and A. Neviani, "A fully integrated differential CMOS LNA for 3-5 GHz ultra wide band wireless receivers," IEEE Microw, Wireless Compon. Lett., vol. 16, no. 3, pp. 134-136, Mar. 2006.
- [10] S. C. Blaakmeer, E. A. Klumperink, D. M. Leenaerts, and B. Nauta, "A wide band noise-canceling CMOS LNA exploiting a transformer," in Proc. IEEE Radio Frequency Integrated Circuits Symp., jun. 2006.
- [11] X. Fan, H. Zhang, and E. Sanchez-Sinencio, "A noise reduction and linearity improvement technique for a differential cascode LNA," IEEE J. Solid-State Circuits, vol.43, no.3, pp. 588-599, Mar. 2008.
- [12] X. Li, T. Brogan, M. Esposito, B. Myers, and K. K. O, "A comparison of CMOS and SiGe LNA's and mixers for wireless LNA application," in Proc. IEEE Custom Integrated Circuits Conf. (CICC), 2001, pp. 531-534.