

An Optimal Design of CMOS Two Stage Comparator Circuit Using Swarm Intelligence Technique

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ABSTRACT

A swarm intelligent based optimization technique named as Flower pollination algorithm (FPA) is applied for the design of the CMOS two stage comparator circuit. The basic idea of FPA mimics the flower pollination process of flowering plants. The input control parameters of FPA improve the exploration and exploitation capabilities of optimization problem. This paper presents the design of a CMOS two-stage comparator circuit using simulation based model called swarm intelligence technique. Simulation results shows that the proposed method is capable to determine the transistor sizes and bias current values of the CMOS comparator. The results obtained from the FPA improved the design performance of comparator in terms of power consumption, MOS transistor area and gain. To investigate the efficiency of proposed approach, comparisons have been carried out with differential evolution (DE) and harmony search (HS) algorithm based circuit design. The performances of FPA based comparator design are better than the previously reported works.

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1. INTRODUCTION

Analog integrated circuit (IC) design is one of challenging task in the growth of modern electronics system. The design of digital circuit is completely automated, and the analog functions are converted into digital value wherever possible. For last few decades, the electronics system design seemed that everything could be digital. However, the real world signals are analog in nature; these signals are communicated through analog circuits [1]. For digital signal processing applications, it is necessary to interface the analog circuit to the system [2]. In recent times, the analog circuit design regaining attention by researchers in the area of system on chip (SoC). The basic concept of SoC is to integrate both analog and digital circuit in a single chip. One of the main challenging tasks in designing SoC is to minimize analog circuit design time. For mixed signal system design, the absence of analog automated synthesis tool to increase the design cycle time.

Deterministic approach for analog circuit design needs good starting point, which can be assigned by analog designer [3-6]. The accuracy of this method is depends on the dc point and the knowledge of analog designer. Then this method is interface with spice engine to enhance the design parameters. However, the deterministic approaches are not suitable for complex circuits [7].

Heuristic based optimization approaches can be used to model the analog circuit design problems. The most popular heuristic methods are local search [8], tabu search [9], and simulated annealing [10].

These techniques were applied to the analog circuit design. These mathematical approaches implemented to form a model with different types of design variables and constraints. However these methods do not guarantee the optimal solution. Meta-heuristics algorithms were proposed to overcome the main issues of heuristic based optimization approaches. These algorithms are inspired from the nature and mainly they mimic the animal hunting behavior towards the food source. Some meta-heuristics approaches used for analog circuit design are particle swarm optimization [11], harmony search algorithm [12] and ant colony optimization [13]. These techniques try to provide the optimal solution to the problem. The swarm intelligence techniques are mostly suitable for complex optimization problem [14-16]. They have better ability to find the global optimal solution in reasonable time. The main motivation of this work is to optimize the transistor size and bias current value to meet the design specification of the CMOS comparator circuit. The simulation-based optimization technique is proposed to optimize the circuit design parameters. In compared with other method the swarm intelligence based method provide the batter results.

The reaming part of this paper is organized as follows: Section 2 describes the comparator circuit structure and design specification. The third section presents the mathematical representation and the operations of salp swarm optimization. The fourth section describes the simulation results and discussion. Finally, the fifth section is the conclusion of work.

2. DESIGN SPECIFICATION AND OBJECTIVE FUNCTION FORMULATION

An optimal design of CMOS comparator has large number of design parameters. The special kind of design procedure required to handle the design variables. The design specifications for the comparator are dc gain, slew rate and power dissipation etc. For comparator design, input bias current, the transistor length and width are considered as the design variables. The relationship between these variables used to implement the design process of circuit. In order to obtain the optimal value of MOS transistor sizes and bias current value, the objective function is developed from the design specifications of the circuits [17]. The objective function of proposed comparator is to minimize the total area of the chip. The circuit structure and configurations of the comparator circuit is shown in Figure 1.

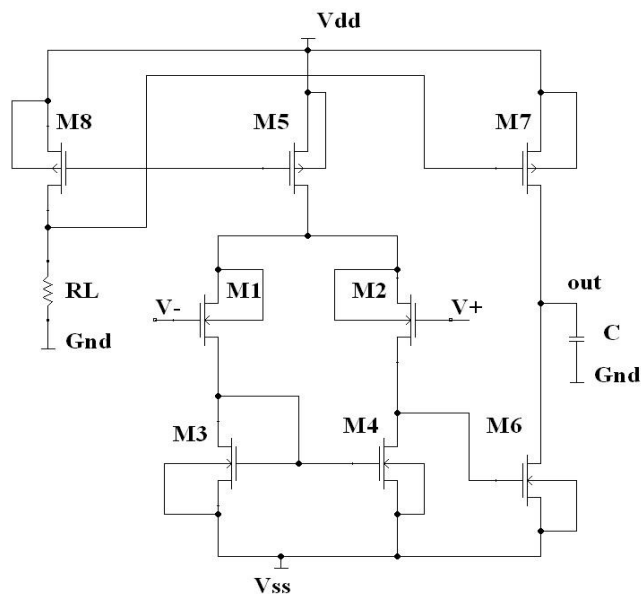


Figure 1. CMOS two stage comparator circuit

2.1. Design Criteria for the CMOS Two-stage Comparator

The basic idea of a comparator circuit is to compare the two input signals (in terms of current or voltage) and output shows which signal is high. The input variables for the design of comparator circuit are given as follows:

V_{DD} and V_{SS} are the positive and negative power supply respectively; V_{tn} and V_{tp} are the NMOS and PMOS threshold voltage respectively; $K'_n = \mu_n \cdot C_{ox}$ and $K'_p = \mu_p \cdot C_{ox}$ are the transconductance parameter of NMOS and PMOS transistors. Where μ_n and μ_p indicates the electron and hole mobility; C_{ox} is the gate oxide capacitance per unit area.

The design steps involved in the comparator circuit are as follows [18]:

Find the range of I_{D7} to satisfy slew rate (SR)

$$SR = \frac{I_{D7}}{C_L} \quad (1)$$

$$\frac{W_6}{L_6} = \frac{2 \cdot I_{DS6}}{K_p [V_{DS6}]^2} \quad (2)$$

$$\frac{W_7}{L_7} = \frac{2 \cdot I_{DS7}}{K_p [V_{DS7}]^2} \quad (3)$$

$$A_{v2} = - \frac{g_{m6}}{g_{ds6} + g_{ds7}} \quad (4)$$

Find out the first stage voltage gain from overall gain

$$A_{v1} A_{v2} = A_v \geq 10000 \quad (5)$$

Find out the current values following through M1, M2, M3 and M4

$$I_{DS1} = I_{DS2} = I_{DS3} = I_{DS4} = I_{DS5/2} \quad (6)$$

Calculate the current I_{DS4} , where

$$I_{DS4} = \frac{(W/L)_4}{(W/L)_6} I_{DS6} \quad (7)$$

$$I_{DS5} = 2I_{DS4} \quad (8)$$

Calculate the current I_{DS7} , where

$$I_{DS5} = \frac{(W/L)_5}{(W/L)_6} I_{DS7} \quad (9)$$

$$I_{DS4} = I_{SD5} / 2 = I_{DS3} \quad (10)$$

$$I_{SD2} = I_{SD1} = I_{SD5} / 2 \quad (11)$$

Find the value of $\frac{W_5}{L_5}$ in order to satisfy the positive ICMR.

$$(W / L)_1 = \frac{[A_{V1} I_{SD1} (\lambda_N + \lambda_P)]^2}{2K_P I_{DS1}} \quad (12)$$

$$V_{SD(SAT)} = V_{DD} - V_{G1(max)} - \sqrt{2I_{DS1} / K_P (W / L)_1} - V_{T1} \quad (13)$$

$$(W / L)_5 = \frac{2I_{DS5}}{K_P [V_{DS5(SAT)}]^2} \quad (14)$$

Find the value of $\frac{W_3}{L_3}$ in order to satisfy the negative ICMR.

$$(W / L)_3 = \frac{2I_{DS3}}{K_P (V_{G1(min)} - V_{SS} - V_{T3} + V_{T1})^2} \quad (15)$$

Find the value of biasing resistor (R_b), where

$$R_b = \frac{V_{SD8} - 0}{I_{DS8}} \quad (16)$$

The cost function of FPA is the given by (i.e. The total chip area of an operational amplifier)

$$CF = \sum_{i=1}^N (W_i \times L_i) \quad (17)$$

Where, N represents the number of transistors, W_i and L_i are the width and length of transistors.

3. PROPOSED FLOWER POLLINATION ALGORITHM (FPA) FOR CMOS TWO STAGE COMPARATOR CIRCUIT OPTIMIZATION

Flower pollination algorithm is a population based meta-heuristics optimization algorithm, which mimics the flower pollination process of flowering plants and the basic structure of FPA is presented in [19]. This algorithm is simple in nature and it has only two search operators namely, the global search operator and the local search operator. These two operators normally used to iteratively update the candidate solution. The mathematical representation of global search operator is expressed as,

$$P_i^{t+1} = P_i^t + \gamma L(\gamma)(P_i^t - g^*) \quad (18)$$

Where P_i^t indicates the solution P_i at t-th iteration, g^* indicates the best solution in the current population, γ represents the scale factor ($\gamma = 0.01$). $L(\gamma)$ indicates the levy flight step size. The general equation of levy distribution when $L > 0$ is follows as,

$$L \propto \frac{\lambda \Gamma(\lambda) \sin(\pi \lambda / 2)}{\pi} \cdot \frac{1}{s^{1+\lambda}}, (s \gg s_0 > 0) \quad (19)$$

Where $\Gamma(\lambda)$ indicates the standard gamma function, s represents the step size.

The mathematical representation of local search operator is expressed as,

$$P_i^{t+1} = P_i^t + \xi(P_j^t - P_k^t) \quad (20)$$

Where P'_j and P'_k indicate two randomly selected solutions, and ξ represents a random number in $[0, 1]$.

The FPA more likely uses the local search operator in order to solve optimization problem. This can be achieved by the probability coefficient (p) which is 0.8 for the local search operator and 0.2 for the global search operator. The Nelder-Mead is a local optimization technique used to improve the local search exploitation of FPA.

The steps of proposed NMFPA are as follows:

Step 1: Control parameter setting: the population size N, the switch probability p, maximum number of iteration and the parameters for the simplex method.

Step 2: Evaluate the N candidate solutions and find the best solution from that.

Step 3: Based on switch probability, generate a new solution using the local search operator or the global search operator. The new solutions are better than current solution then update the best solution.

Step 4: Select the n+1 best solution and form an initial simplex using Nelder-Mead method. Then execute m times and replace the previous selected n+1 solution. Now update the current best solution.

Step 5: Continue iterations from step 3 until the end condition satisfied.

The main aim of this paper is to find the length and width of the transistor by utilizing the FPA. The input specification and its range are shown in Table 1.

Table 1. Design Parameters, Technology and Constant values of Two-Stage Operational Amplifier

Inputs, Technology	Values
V_{DD}	1.8 V
V_{SS}	-1.8 V
V_{ip}	-0.43 V
V_{tn}	0.48 V
K_n	345 ($\mu A/V^2$)
K_p	55 ($\mu A/V^2$)
Technology	0.18 μm

4. SIMULATION RESULT

This section describe the simulation result of FPA based CMOS comparator circuit design. The proposed hybrid optimization algorithm is constructed using MATLAB for the design of CMOS comparator. The design parameters and design constraints are considered as the input variable for optimization algorithm. The constant circuit design variables are taken from model parameter called GPDK 180nm technology. The main objective is aimed to minimize the total chip size of CMOS comparator circuit. The result obtained from the flower pollination algorithm based comparator design is compared with existing methods like Differential Evolution (DE) and Harmony Search (HS) algorithm [20]. The input variables and their values are given in Table 1, in order to define the input range of an optimization problem. The comparator cost function is aimed to minimize the chip area less than 300 μm^2 . The simulation results show that the least chip area of 36.77 μm^2 . An optimal transistor dimension values of the CMOS comparator are given in Table 2. To evaluate the efficiency of the proposed optimization technique is compared with other techniques called differential evolution and harmony search shown in Table 3 Figure 2 show the efficiency of proposed algorithm in terms of power dissipation. The simulation results show that the proposed optimization technique is most suitable for simple analog circuit design.

Table 2. Optimal transistor dimension for CMOS two stage comparator

Design parameters	Values	Units
W_1/L_1	23.24/0.18	($\mu m/\mu m$)
W_2/L_2	23.24/0.18	($\mu m/\mu m$)
W_3/L_3	2.5/0.18	($\mu m/\mu m$)
W_4/L_4	2.5/0.18	($\mu m/\mu m$)
W_5/L_5	5.8/0.18	($\mu m/\mu m$)
W_6/L_6	47/0.18	($\mu m/\mu m$)
W_7/L_7	87.5/0.18	($\mu m/\mu m$)
W_8/L_8	12.5/0.18	($\mu m/\mu m$)
R_b	88	kohm

Table 3. Design Specifications Result of the CMOS Two Stage Comparator

Design criteria	Specifications	DE	HS	Proposed method
Load capacitance (pF)	≥ 10	10	10	12
Unity gain bandwidth (MHz)	≥ 10	16.055	17.255	18.43
Gain (dB)	> 80	82.424	82.932	85.8
Slew Rate (V/ μ s)	≥ 10	160	160	120
$V_{ic_{min}}$ (V)	≥ -1.65	-1.6042	-1.6146	-1.2160
$V_{ic_{max}}$ (V)	≤ 1.65	1.6458	1.5938	1.1934
CMRR (dB)	> 85	87.4715	87.8223	89.42
Area (μm^2)	< 300	8200	265	36.77
Power dissipation (μW)	≤ 1000	511	508	309

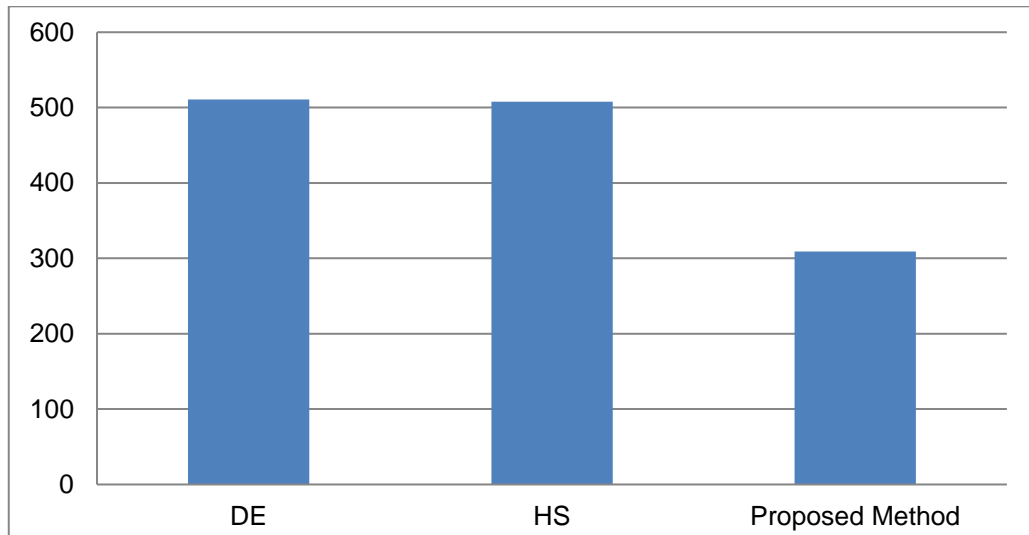


Figure 2. Power dissipation of two stage comparator circuit

5. CONCLUSION

A new swarm intelligent technique for determining the transistor sizes, input bias current and other parameters of CMOS comparator is presented. Flower pollination algorithm (FPA) has shown its exploration and exploitation capability in finding the optimal design parameters in multidimensional search space. At the same time the proposed technique reduces the chip area, power dissipation and increases the DC gain of CMOS comparator. Simulation result demonstrates that the proposed algorithm successfully met the circuit design specification. The simulation results show that the FPA optimization method is efficient method for the design of simple analog circuits.

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